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A 0.58 mm2 CMOS reconfigurable sigma delta ADC for mobile WiMAX receiver[1]

Un CMOS 0.58 mm2 reconfigurable sigma delta CAD para receptor móvil WiMAX[2]

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Abstract

Objective: In this work the design of a fourth-order reconfigurable sigma delta analog-to-digital converter (ΣΔ ADC) for 5 MHz, 7 MHz or 10 MHz channel bandwidths is presented. *Materials and methods:* Our design technique aims to keep the same ADC architecture in response to multi-band and multi-mode aspects of the mobile WiMAX standard. To this end, we set each sampling frequency corresponding to each channel bandwidth, in order that the same OSR value would be kept for the different channel bandwidths. This technique is intended to optimize the power and area of the ADC to efficiently cover varying channel bandwidths. Moreover, we use the pole placement method to calculate the optimized filter coefficients of continuous-time sigma-delta (CT ΣΔ) ADC. *Results and discussion:* Over 5 MHz, 7 MHz and 10 MHz channel bandwidths, the ADC achieved 72.89 dB, 67.26 dB and 66.47 dB peak SNR values, respectively, and a dynamic range of 73.5 dB, 69.47 dB and 66.5 dB, respectively, with only 28 mW, 28.2 mW and 28.6 mW power consumption, respectively. *Conclusions:* We achieved the design and implementation of the proposed reconfigurable ADC intended for use with the mobile WiMAX standard. Moreover, the results obtained are satisfactory and are in accordance with theoretical expectations.

Keywords: Continuous-Time ΣΔ ADC, Mobile WiMAX, Reconfigurable ADC, Regulated telescopic OTA, Feedback DAC.

Resumen

Objetivo: en este trabajo se presenta el diseño de un convertidor analógico a digital reconfigurable Sigma Delta (ΣΔ CAD) de cuarto orden para anchos de banda de canal de 5MHz, 7MHz o 10MHz. *Materiales y métodos:* nuestra técnica de diseño tiene como objetivo mantener la misma arquitectura de CAD en respuesta a los aspectos multibanda y multimodo del estándar móvil WiMAX. Para este fin, establecemos cada frecuencia de muestreo correspondiente a cada ancho de banda del canal, para que se mantenga el mismo valor OSR para las diferentes anchuras de banda del canal. Además, utilizamos el método de colocación de polos para calcular los coeficientes de filtro optimizados de Continuous-Time Sigma-Delta (CT ΣΔ) CAD. *Resultados y discusión:* El ancho de banda de canal de 5MHz, 7MHz y 10MHz alcanzó valores de SNR de pico de 72.89dB, 67.26dB y 66.47dB respectivamente, y un rango dinámico de 73.5dB, 69.47dB y 66.5dB, respectivamente, con solo 28mW, 28.2mW y 28.6mW consumo de energía respectivamente. *Conclusiones:* Se logró el diseño y la implementación del ADC reconfigurable propuesto para su uso en el estándar móvil WiMAX. Además, los resultados obtenidos son satisfactorios y están de acuerdo con las expectativas teóricas.

Palabras clave: Continuo-tiempo ΣΔ CAD, móvil WiMAX, CAD reconfigurable, AOT telescópica regulada, CDA de retroalimentación.

1. Introduction

WiMAX (Worldwide Interoperability for Microwave Access) embodies the IEEE 802.16 family of standards that provision wireless broadband access. With the IEEE 802.16e−2005 mobility amendment, WiMAX promises to address the ever-increasing demand for mobile high-speed wireless data in fourth-generation (4G) networks [1-2]. In addition, mobile broadband wireless networks, such as mobile WiMAX, have been designed to support several features, incliding quality of service or enhanced data protection mechanisms, in order to provide true access to real-time multimedia applications [3]. Further, mobile WiMAX uses a new physical layer radio access technology called Orthogonal Frequency Division Multiple Access (OFDMA) as the multiplexing technique in uplink and downlink [4].

With the development of wireless communication systems, there has been increasing demand for low cost and low power ADCs. ΣΔ ADCs are ideally suited to such applications. In fact, while oversampling ADCs have proven useful in high resolution and wide frequency applications, Nyquist ADCs are more competitive for these applications [5]. In addition, the input signal to the ΣΔ ADC is oversampled at a much higher frequency than the Nyquist rate. "This means that the effective bandwidth of the signal constitutes a negligible portion of the whole band. Noise shaping techniques are used to reduce the power spectrum of noise in the effective bandwidth of the signal." Note that in this case, the quantization error is also treated as noise. Several implementations of the discrete-time and continuous-time ΣΔ ADCs have been presented in the literature [6-7].

The need for low power ADC is increasing as CMOS technology is scaling down. CT ΣΔ ADCs promise lower power consumption than discrete-time ADCs [8]. In addition, a CT ΣΔ ADC is an attractive choice of ADC implementation as it possesses inherent anti- aliasing filter characteristics and relaxed requirements on integrators, thus eliminating the need for additional filtering and sampling circuitry, thus mitigating power consumption. They also do not require complex switching and clocking mechanism, thus paving the way for very high OSR [9]. However, they are less robust against jitter effects and excess loop delay compared with their discrete-time counterparts [10]. For this reason, we proposed a fourth-order reconfigurable CT ΣΔ ADC intended for use in the mobile WiMAX standard. In addition, our design technique aims to maintain a specific ADC architecture in response to the multi-mode and multi-band aspects of the mobile WiMAX standard.

The remainder of this paper is organized as follows. The reconfigurable CT ΣΔ ADC architecture is described in Section 2. Section 3 addresses the reconfigurable ADC implementation. Section 4 presents the post-layout simulation. Finally, the main conclusions of this study are drawn in Section 5.

2. The proposed reconfigurable CT ΣΔ ADC architecture

The proposed CT ΣΔ ADC architecture is considered for a multi-band and multi-mode system in 5 MHz, 7 MHz or 10 MHz channel bandwidths (BW). It is a reconfigurable and programmable ADC, which aims to optimally cover bandwidth and resolution ranges and to optimize power and area for a specific application using the same ADC architecture. The reconfigurable ADC is based on bandwidth reconfiguration by dynamically adapting a sampling frequency and an over- sampling ratio (OSR) [11]. In fact, the main purpose of our methodology is for designing a reconfigurable CT ΣΔ ADC that efficiently covers varying channel bandwidths by configuring the ADC to the proper architecture for each channel bandwidth.

The purpose of our design technique is to keep a specific ΣΔ ADC architecture in response the multi-band and multi-mode aspects of the WiMAX standard. To this end, we set each sampling frequency corresponding to each channel bandwidth, so that we keep the same OSR value for each channel bandwidth. Moreover, we use a single-bit quantizer for each channel bandwidths. This technique is intended to optimize power and area compared to ΣΔ ADCs that consist of two or three cascaded stages [12].

The over-sampling ratio is given by:

$$OSR = \frac{F_s}{2 \times F_b} \tag{1}$$

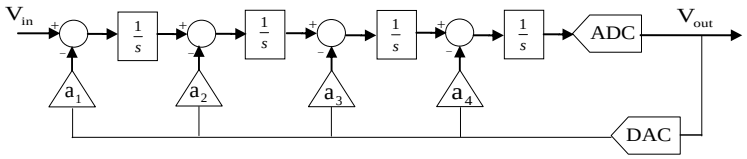
Where F_s is the sampling frequency and F_b is the signal bandwidth. The theoretical modulator signal-to-noise ratio is expressed as [13]:

$$SNR_{th} = 10\log\left(\frac{3}{2} \times \left(\frac{2L+1}{\pi^{2L}}\right)\left(2^n - 1\right)^2 OSR^{2L+1}\right) \tag{2}$$

Where L, OSR and n are the ADC order, the over-sampling ratio and the quantizer bitness, respectively.

To increase immunity to interferences, a reconfigurable CT ΣΔ ADC with a feedback loop architecture should be used since its signal transfer function (STF) has a faster roll-off in out-of-channel frequencies in comparison to feedforward loop architectures [14]. The stabilization of the modulator transfer function is performed by using a loopback input at each filter stage [15]. A conventional fourth-order feedback low-pass CT ADCs with a single-bit quantizer is shown in Figure 1 [16]. The proposed CT ΔΣ ADC architecture consists of a mono-bit quantizer, operating at 125 MHz, 175 MHz and 250 MHz with an OSR of 25.

Figure 1. Reconfigurable ADC block diagram.



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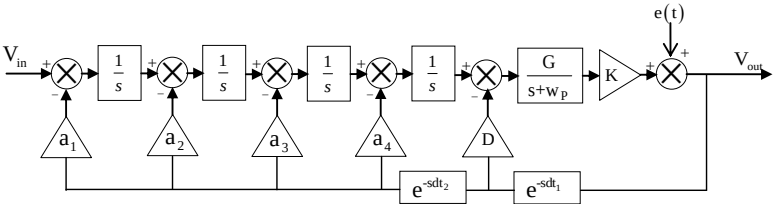
We used the pole placement method introduced in [17], a linearization technique of CT ΣΔ loop, to calculate and analyze the noise shaping transfer function (NTF) of the CT ADC according to the loop gain variation. This method aims to calculate the optimized coefficients of the CT filter to achieve desired noise shaping. The block diagram describing the architecture of fourth-order feedback ΣΔ ADC is shown in Figure 2. As seen this figure, the CT ADC has a delay compensation system for the signal propagation delay in the internal ADC and feedback digital analog converters. The ADC correction system was achieved by introducing two fixed deadlines (dt_1 and $dt_{2)}$ and looping D.

Figure 2. Architecture description of the flexible ADC block diagram.



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The analytical expression of the linearized noise shaping transfer function can be written as:

$$NTF(s)=\frac{s^4(s+w_P)}{s^4(s+w_P)+Ge^{-sdt_1}Ds^4+Ge^{-s(dt_1+dt_2)}(a_1+a_2s+a_3s^2+a_4s^3)} \quad (3)$$

Where w_P is the cut-off frequency and the gain K of the linearized model is set to one for calculation of the loop coefficients. Moreover, to numerically calculate the loop coefficients, it is sufficient to select the desired CT ΣΔ noise shaping. The Butterworth or Chebyshev filtering functions are often preferred. Knowing the analytical expression of the linearized NTF and the desired pole position, it becomes easy to calculate the corresponding loop coefficients. The coefficients optimized with the pole placement method are summarized in Table 1. Table 2 lists the WiMAX ADC specifications.

Table 1. Optimized CT filter coefficients.

Coefficient	Value
a_1	1
a_2	4.6
a_3	14.7
a_4	21.1
D	23.2

Source: Authors own creation.

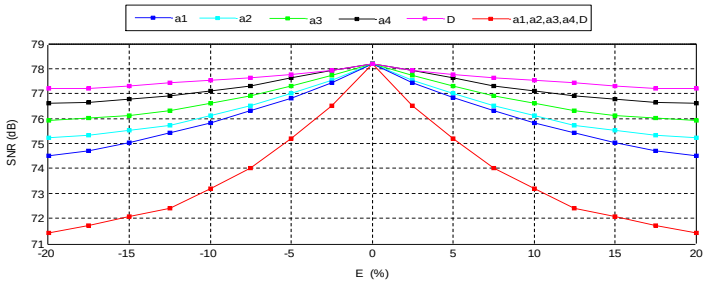
Table 2. Specifications of mobile WiMAX ADC.

Channel bandwidth (MHz)	Sampling frequency (MHz)	OSR	Resolution (bits)
5	125	25	11.4
7	175	25	11.1
10	250	25	11.1

Source: Authors own creation.

Deviation of the CT filter coefficients can affect the ADC signal-to-noise ratio. Figure 3 depicts the ADC SNR deviations versus the errors (E) of the CT filter coefficients (a_1, a_2, a_3, a_4 and D) for 5 MHz channel bandwidth. Obviously, at E=0, the SNR is at the maximum.

Figure 3. SNR versus the errors of CT filter coefficients.



Source: Authors own creation.

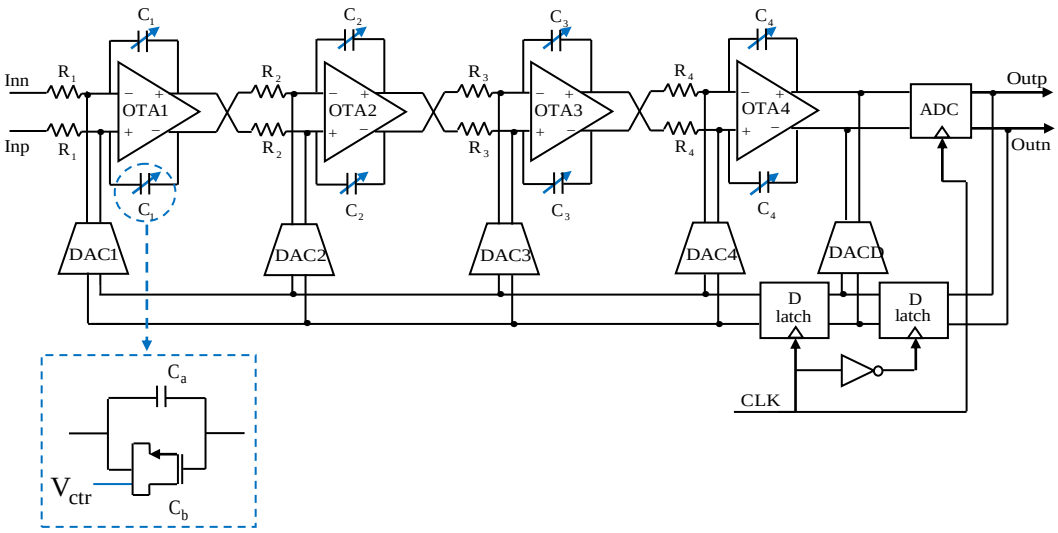
The system becomes less stable when the error of the CT filter coefficients exceeds ±10%, representing the tolerable error limit, which proves the robustness of the pole placement method.

3. Design method of the reconfigurable CT ΣΔ ADC

The loop filter utilizing CT ΣΔ ADC was achieved with an active-RC op-amp circuit as shown in Figure 4. This implementation allows the benefits of high linearity, high output signal swing, and a good virtual ground for the digital analog converters (DAC) in the ADC

feedback [18]. The CT-filter coefficients are implemented using current-steering DACs with NRZ feedback [19]. The excess loop delay effect is typically a constraint in the CT ΣΔ ADC. Hence, an extra feedback branch between the output and the input to the quantizer (DAC D in Figure 4) and two D latches were used in both stages in order to avoid excess loop delay effect [20].

Figure 4. Block diagram of the reconfigurable CT ΣΔ ADC.



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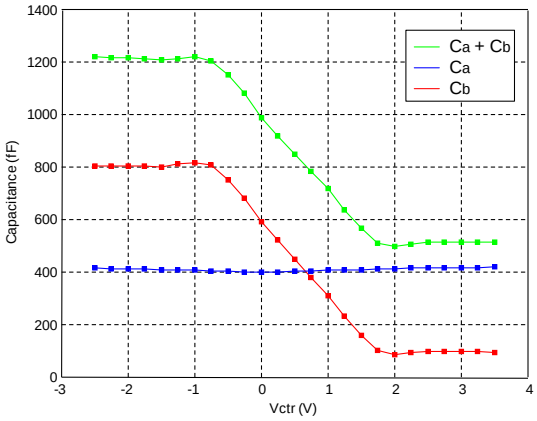
The CT ΣΔ ADC operates with three different sampling frequencies, which are applied to the two D latches and the comparator. Thus, each sampling frequency corresponds to these RC integration constants. For this reason, we used variable capacitances. Each integrator capacitance is made up of two capacitances sum C_a and C_b. In fact, C_a and C_b represent the MIM capacitor and variable capacitor, respectively, in an NMOS transistor where the drain and the source are connected together and controlled by the control voltage (V_{ctr}). Figure 5 shows the MIM and NMOS gate capacitance values versus V_{ctr}. Moreover, the capacitor built as a parallel connection of MIM and NMOS gate capacitances versus V_{ctr} is shown in the same figure. The capacitance decreases from 1.22pF to 0.5pF over the V_{ctr} range -1V to 2V.

Given the above overview of the proposed structure, we can easily examine its various blocks in details in the following subsections. In particular, we presented transistor-level performance of the Regulated Telescopic Operational Transconductance Amplifier (OTA), the comparator, and the clock generator.

Figure 5. Capacitance values versus Vctr.



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3.1 Regulated Telescopic OTA Design

Several fundamental issues arise when selecting an optimal architecture for the OTA circuit. This choice aims at achieving both large gain and a large bandwidth performance. We used the Regulated Telescopic OTA instead of the Telescopic OTA in order to obtain increased DC gain without changing the gain-bandwidth product (GBW). In fact, the Regulated Telescopic OTA is a version of the simple Telescopic circuit with the gate voltage of the cascade transistor being controlled by a feedback amplifier [21]. The feedback is applied around the cascade transistor in order to improve the gain. This feedback is in fact a parallel-series, causing the output impedance to rise with the feedback gain. The gain increases proportionally. Figure 6 shows the Regulated Telescopic OTA circuit. Despite adding a feedback amplifier, the voltage swing of the Regulated Telescopic OTA at the output node was reduced and the layout area increased, compared to the Telescopic OTA.

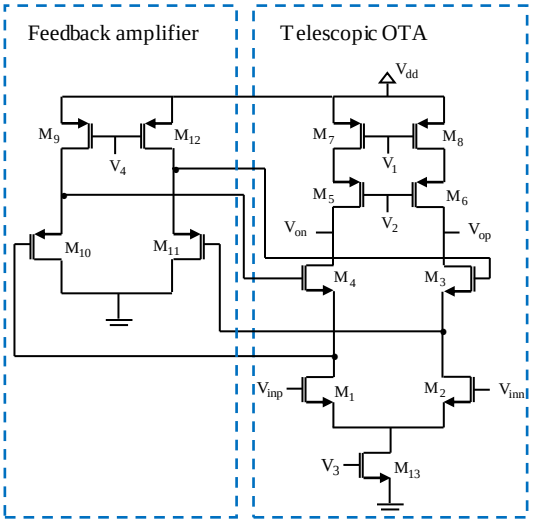
The open loop gain (A_V) for the Regulated Telescopic OTA circuit and the GBW are given respectively by the following equations:

$$A_v = g_{m1}((g_{m4}g_{m10})ro_4\left(ro_{10}//ro_9\right)ro_1)//\left(g_{m5}ro_5ro_7\right) \tag{4}$$

$$GBW = \frac{g_{m1}}{2\pi\left(C_{DB2}+C_L+C_{GD2}\right)} \tag{5}$$

Where g_{mi} is the transconductance of M_i transistor for I = (1, 4, 5, 10), ro_i is the drain-source resistance of M_i transistor for i = (1, 4, 5, 7, 9, 10), C_{GD2}, C_{DB2} and C_L are the drain gate capacitance, the bulk drain capacitance of the M_2 transistor and the load capacitance at the output node, respectively.

Figure 6. Regulated Telescopic OTA circuit.



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According to [22], we applied the following constraint:

$$\frac{1}{A_v} \leq \frac{1}{2} q \tag{6}$$

Where q is the quantization step of the CT ΣΔ ADC. It is calculated as follows:

$$q = \frac{V_{Full\_scale}}{2^N} \tag{7}$$

Where the ADC full scale level (V_{Full_scale}) is equal to 13 dBm and the ADC resolution (N) is equal to 11bits [16]. In this case, we assume the overall gain A_v is greater than 60 dB. In [22], it is mentioned that:

$$GBW \geq 3F_S \tag{8}$$

The output frequency response of the Regulated Telescopic OTA is plotted in Figure 7. The Regulated Telescopic OTA has a DC gain of 66 dB, a large GBW of 862 MHz and a phase margin of 58 degrees. The Regulated Telescopic OTA performance measures are summarized in Table 3.

Figure 7. Gain and phase curve.

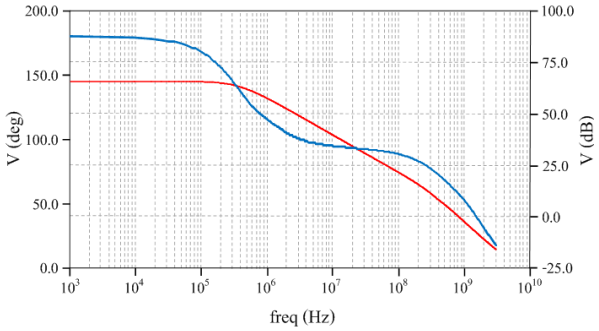

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Table 3. Regulated telescopic OTA performances.

Specifications	Values	
	Pre-layout simulation	Post-layout simulation
Output Load (pF)	1	1
DC gain (dB)	69.15	66
GBW (MHz)	870	862
Phase margin (degrees)	60	58
CMRR (dB)	51	49.4
Slew rate (V/µs)	±351	±349
Settling time (ns)	14,24	14,3
Output-voltage swing (V)	-1.5 to 1.5	-1.2 to 1.2
Supply voltage (V)	0 - 3.3	0 - 3.3
Power consumption (mW)	6.22	6.24
Layout area (μm^2)	-	(221×202)

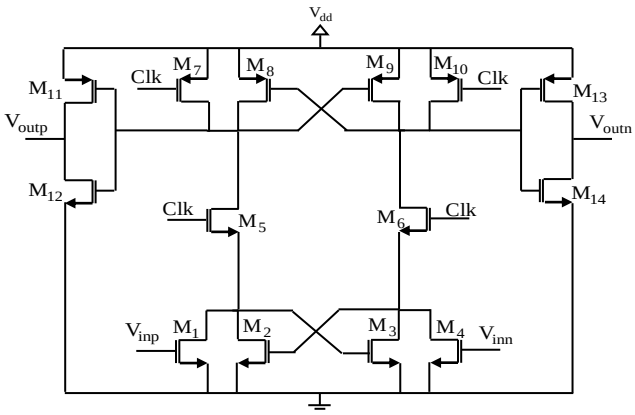
Source: Authors own creation.

3.2 Latched Comparator

A latched comparator was used here to act as a single-bit quantizer to convert an analog signal into a digital signal [23]. Figure 8 depicts the latched comparator architecture where the speed should be adequate to achieve the desired sampling rate, input offset, input referred noise, and hysteresis. The offset and noise at the comparator input would be omitted by the feedback loop of the CT ΣΔ ADC.

Post-layout simulation of the latched comparator verified that the propagation delay was approximately 1.2 ns, 1.16 ns and 1.1 ns for 125 MHz, 175 MHz, and 250 MHz clock frequencies, respectively, and the power consumption was only 16 µW. Additionally, the latched comparator occupied a layout area of (72×62)μm^2.

Figure 8. Latched comparator circuit.



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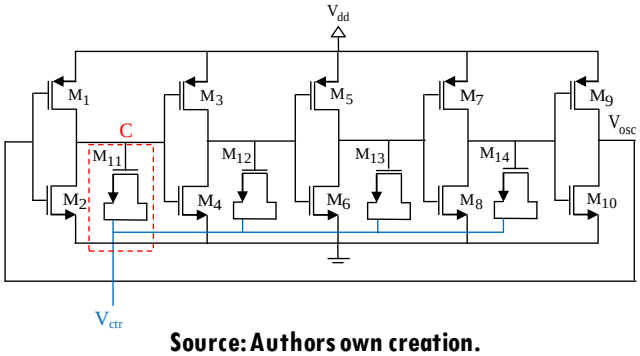
3.3 Clock Generator

The CMOS ring oscillator architecture is made up of five stages of inverters in series separated by capacitors and looped between each structure [24]. The clock generator is used here in order to generate different sampling frequencies for the CT ΣΔ ADC such as 125 MHz, 175 MHz and 250 MHz. Therefore, we used the CMOS ring oscillator architecture with variable capacitors as shown in Figure 9. Moreover, the ring oscillator exhibited a rise time of 0.2 ns, a power consumption of 19 µW, and layout area of (70×44)µm^2.

Figure 9. Clock generator circuit.



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The oscillating frequency (f_{osc}) is given by the following equation:

$$f_{osc} = \frac{1}{n\left(tp_{HL} + tp_{LH}\right)} \tag{9}$$

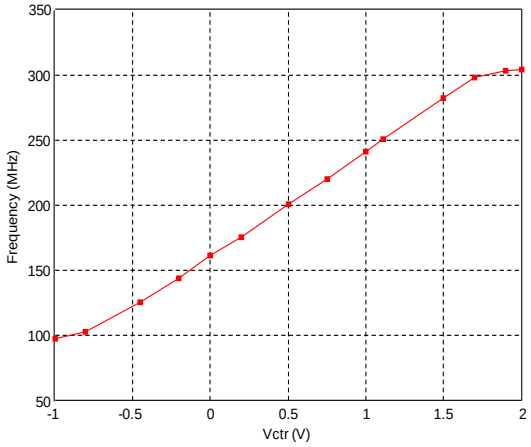
Where n is the number of stages, tp_{HL} is the fall time and tp_{LH} is the rise time. Further, tp_{HL} and tp_{LH} are given respectively in (7) and (8).

$$tp_{HL} = \frac{4C}{K_P \frac{W_P}{L_P} V_{dd}} \tag{10}$$

$$tp_{LH} = \frac{4C}{K_N \frac{W_N}{L_N} V_{dd}} \tag{11}$$

Where K_P and K_N are the intrinsic transconductance of the PMOS and NMOS transistors, respectively, and C is the value of the variable capacitor. In fact, the variable capacitor C is an NMOS transistor whose drain and source were connected together and controlled by the control voltage (V_{ctr}). Figure 10 depicts the oscillating frequency versus V_{ctr}. The oscillating frequency varies from 98 MHz to 304 MHz over the V_{ctr} range -1 V to 2 V.

Figure 10. Post-layout simulation for oscillating frequency versus V_{ctr}.



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3.4 SNR Versus Normalized RC Time Constant

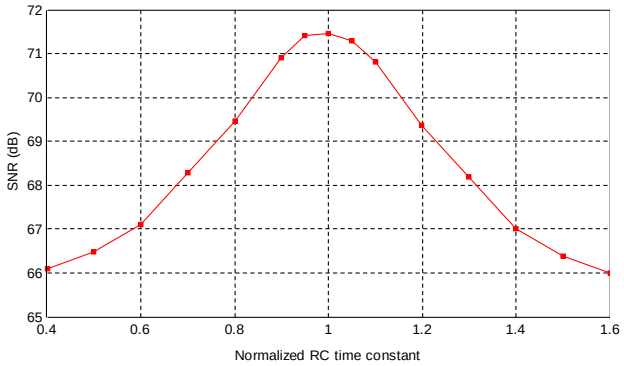
The integrator represents the main building block in CT ΣΔ ADC. The transfer function of the CT integrator used in Fig. 4 is given by:

$$H(s) = \frac{k_i}{sT_s'} \tag{12}$$

for i = (1, 2, 3, 4), where T'_S has a nominal value of T_S, the system clock period. If the integrator time k_i/T'_S deviates from its nominal value, the SNR performance degrades. For this to be proven, Figure 11 presents the post-layout simulated SNR performance of the Flexible CT ΣΔ ADC versus the normalized RC time constant associated with the loop filter.

The x axis is T's/Ts, the normalized time constant, and the y axis is the post-layout simulated flexible ADC SNR. The CT ΣΔ ADC becomes less stable when the RC time constant decreases below 0.8 and increases above 1.2.

Figure 11. SNR versus normalized RC time constant.



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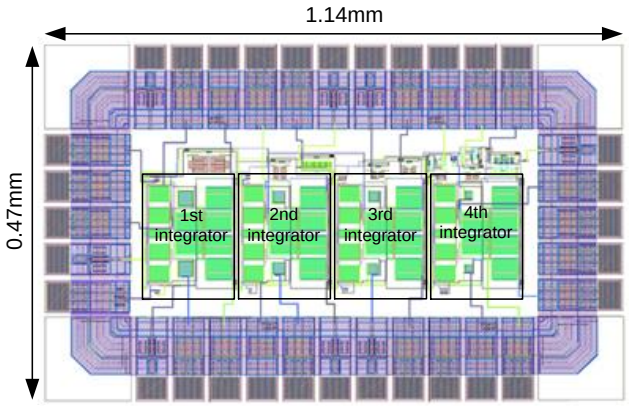
4. Post-Layout Simulation Results

The proposed reconfigurable fourth-order CT ΣΔ ADC was implemented in AMS 0.35µm CMOS process and simulated using the Cadence tool. The reconfigurable ADC samples the signals at 125 MHz, 175 MHz and 250 MHz with respectively 5 MHz, 7 MHz and 10 MHz channel bandwidths, respectively, and the total power consumption is 28 mW, 28.2 mW and 28.6 mW, respectively. The layout of the reconfigurable ADC is shown in Figure 12. This occupies an area of (1.14×0.47)mm^2, including bonding pads.

Figure 12. Layout of the fourth-order flexible CT ΣΔ ADC.



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The post-layout simulation output spectrum of the reconfigurable fourth-order CT ΣΔ ADC for 5 MHz, 7 MHz and 10 MHz channel bandwidths, at a sampling frequencies of 125 MHz, 175 MHz and 250 MHz, respectively, with 16384 samples and an OSR of 25 is shown in

Figure 13. It reveals the SNR values of approximately 71.47 dB, 67.24 dB and 66.37 dB, over channel bandwidths of 5 MHz, 7 MHz and 10 MHz, respectively. In addition, Figure 13 provides transistor level SNR values of approximately 74.8 dB, 71 dB and 70 dB, over channel bandwidths of 5 MHz, 7 MHz and 10 MHz respectively.

Figure 13. Post-layout and transistor level output spectrum of the flexible CT ΣΔ ADC for (a) BW=5 MHz, F_{IN}=0.625 MHz, (b) BW=7 MHz, F_{IN}=0.875 MHz and (c) BW=10 MHz, F_{IN}=1.25 MHz.

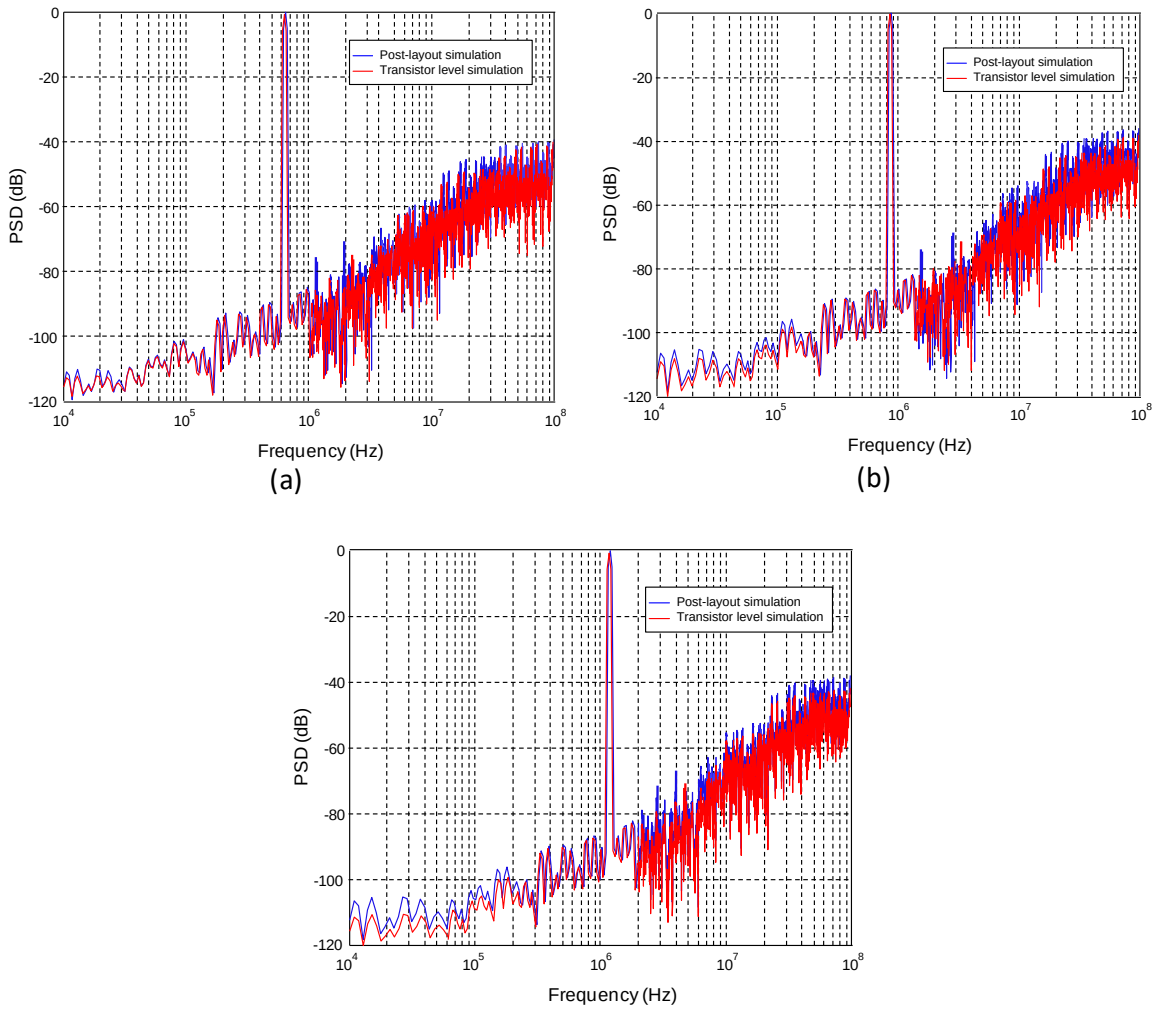

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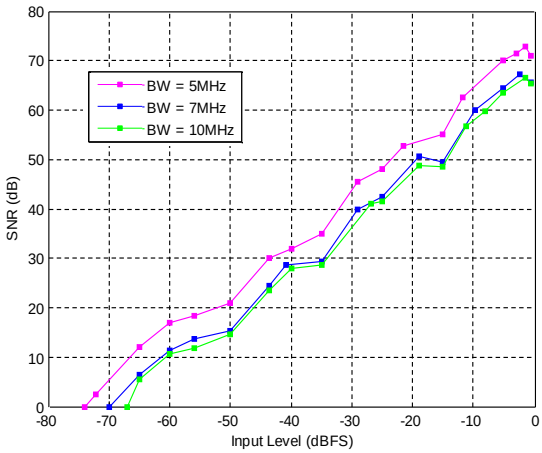
Figure 14 shows the SNR versus input signal amplitude over 5 MHz, 7 MHz and 10 MHz channel bandwidths. The reconfigurable CT ΣΔ ADC achieves 72.89 dB, 67.26 dB and 66.47 dB peak SNR and 73.5 dB, 69.47 dB and 66.5 dB dynamic range, respectively. The signal-to-noise and distortion ratio (SNDR) versus input signal amplitude is shown in Figure 15. It reveals peak SNDR values of 70.79 dB, 64.96 dB and 64.27 dB over channel bandwidths of 5 MHz, 7 MHz and 10 MHz, respectively. The flexible CT ΣΔ ADC performances measures are listed in Table 4. Table 5 summarizes the performance of the proposed reconfigurable CT

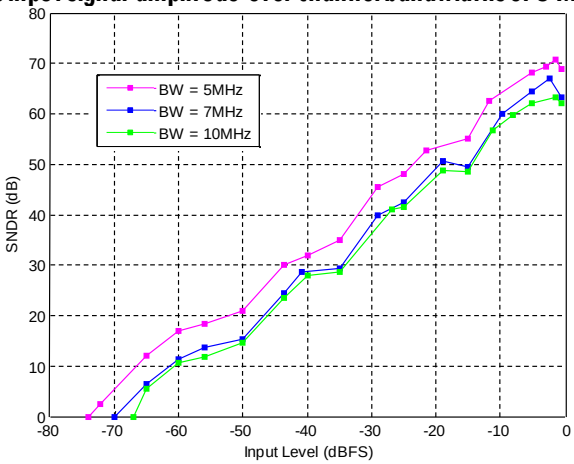
ΣΔ ADC in comparison with other CT ΣΔ ADCs presented recently. Relying on this comparison table, the proposed CT ΣΔ ADC achieves a small FOM of approximately 1.98 pJ/Conv, 2.21 pJ/Conv and 2.43 pJ/Conv over channel bandwidths of 5 MHz, 7 MHz and 10 MHz, respectively.

Figure 14. SNR versus input signal amplitude over 5 MHz, 7 MHz and 10 MHz channel bandwidths.



Source: Authors own creation.

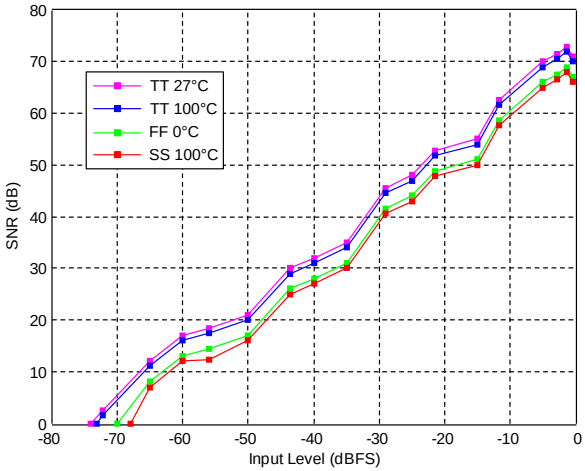
Figure 15. SNDR versus input signal amplitude over channel bandwidths of 5 MHz, 7 MHz and 10 MHz.



Source: Authors own creation.

The SNR versus input signal amplitude over a 5 MHz channel bandwidth was analyzed in different process corners and temperature variations such as TT at 27°C, TT at 100°C, FF at 0°C and SS at 100°C. The results for all process corners and temperature variations are shown in Figure 16. The SS corner at 100°C gives the worst result where, the peak SNR dropped to approximately 4.7 dB.

Figure 16. Process corners and temperature variations post-layout simulation for SNR versus input signal amplitude over a 5 MHz channel bandwidth.



Source: Authors own creation.

Table 4. Reconfigurable CT ΣΔ ADC performances measures.

Specifications	Values					
	Pre-layout simulation			Post-layout simulation		
Sampling Frequency [MHz]	125	175	250	125	175	250
Signal Bandwidth [MHz]	2.5	3.5	5	2.5	3.5	5
Peak SNR [dB]	75.14	72.2	71.45	72.89	67.26	66.47
Peak SNDR [dB]	74.9	71.9	68.15	70.79	67	63.17
ENOB [bits]	12.14	11.65	11.02	11.46	10.83	10.2
Dynamic Range [dB]	75.75	74.41	68.18	73.5	69.47	66.5
FOM [pJ/Conv]	1.22	1.25	1.37	1.98	2.21	2.43
Power Consumption [mW]	27.7	28.17	28.57	28	28.2	28.6
Supply Voltage [V]	0 - 3.3			0 - 3.3		
Process [µm]	0.35			0.35		
Layout Area [mm^2]	-			0.58		

Source: Authors own creation.

5. Conclusions

In this work, the design of a fourth-order reconfigurable CT ΣΔ ADC intended for use in the mobile WiMAX standard was achieved. Our design technique aimed at keeping a specific ADC architecture in response to multi-band and multi-mode aspects of the mobile WiMAX

standard for 5 MHz, 7 MHz and 10 MHz channel bandwidths. For this reason, a sampling frequency was set for each channel bandwidth so that the same OSR value was kept for different channel bandwidths. In addition, the pole placement method was used to calculate the optimized coefficients of the CT filter. Both of the architecture and the main building blocks of the fourth-order feedback low-pass CT ΣΔ ADC with a single-bit quantizer were presented and designed. The reconfigurable ADC die chip occupies an area of 0.58 mm^2 and achieves 72.89 dB, 67.26 dB and 66.47 dB peak SNR values. The power consumption is approximately equal to 28 mW using a 3.3 V supply voltage.

Table 5. Performance comparisons of reconfigurable ADC with other designs

Parameters	This work			[25]	[26]	[27]
Sampling frequency [MHz]	125	175	250	100	100	640
Signal Bandwidth [MHz]	2.5	3.5	5	2	3	10
Peak SNR [dB]	72.89	67.26	66.47	-	-	76
Peak SNDR [dB]	70.79	67	63.17	67.7	57.8	70
ENOB [bits]	11.46	10.83	10.2	10.9	9.31	11.3
Dynamic Range [dB]	73.5	69.47	66.5	-	58	77
FOM [pJ/Conv]	1.98	2.21	2.43	8.9	3.1	1.16
Power consumption [mW]	28	28.2	28.6	68	11.8	60
Supply Voltage [V]	0 - 3.3			1.8	1.8	-
Process [µm]	0.35			0.18	0.18	0.18
Layout Area [mm^2]	0.58			3.2	1.67	-

Source: Authors own creation.

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