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Capacitors placement in distribution systems with nonlinear load by using the variables' inclusion and interchange algorithm

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Abstract
This work presents a substantial improvement of the variables' inclusion and interchange algorithm (VIIA) for capacitors placement that considers circuits with harmonic distortion. Several load states are considered, and fixed and switched capacitors are employed in optimization. All the pertinent constraints of voltage magnitude, total harmonic distortion, individual harmonic distortion, and of overstress of capacitors are implemented. The here defined global harmonic-distortion index states the distance to the feasibility or the unfeasibility of a solution with respect the harmonic distortion constraints. The inclusion in the sequential quadratic programming sub-problem of an inequality linear constraint on this global harmonic-distortion index, allows the determining of solutions that comply with the harmonic distortion related constraints. A comparison of the solutions of various examples obtained by the presented method with the best solutions obtained by the Matlab's genetic algorithm shows the effectiveness of this method.

Keywords: capacitors; harmonics; distribution systems; optimization algorithms

Ubicación de capacitores en sistemas de distribución con carga no lineal mediante el algoritmo de inclusión e intercambio de variables

Resumen
Este trabajo presenta una mejora sustancial del algoritmo de inclusión e intercambio de variables (VIIA) para ubicación de capacitores. Son considerados varios estados de carga y se emplean capacitores fijos y controlados en la optimización. Todas las restricciones pertinentes de distorsión total de armónicos, distorsión individual de armónicos y de sobrecarga de capacitores son implementadas. El índice de distorsión armónica global que aquí se define, establece la distancia a la factibilidad o no factibilidad de una solución con respecto a las restricciones de distorsión armónica. La inclusión en el sub-problema de programación cuadrática secuencial, de una restricción lineal de desigualdad sobre este índice global de distorsión armónica, permite determinar soluciones que cumplen con las restricciones relacionadas a la distorsión armónica. Una comparación de las soluciones obtenidas para varios ejemplos por el método presentado con las mejores soluciones obtenidas por el algoritmo genético de Matlab, muestra la efectividad de este método.

Palabras clave: capacitores; armónicos; sistemas de distribución; algoritmos de optimización.

1. Introduction

Capacitors are used in distribution systems in order to improve the power factor, to reduce the losses, and to improve the voltage profile of the circuits. The correct placement and sizing of the capacitors on circuit's buses, as well as their control in time are very important to obtain maximum benefits.

On the other hand, it is known that the presence of capacitors in a circuit contaminated by harmonics can bring the appearing of resonances. This phenomenon is responsible for the magnification of the harmonic distortion indices and the possible overload of capacitors.

Masoum [1] presents an iterative algorithm for the optimal sizing and placement of fixed and switched capacitor banks. The method combines the maximum sensitivities selection of candidate nodes with local variations, but do not assure optimal solution. Two new contributions are proposed

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by Masoum [2,3]. The first employs a fuzzy-sets approach for selecting the optimal placement and sizing of fixed capacitors. The second, presents a genetic algorithm (GA) for the power quality improvement and optimal placement and sizing of fixed capacitors.

Yu [4] presents a particle swarm optimization (PSO) approach to optimal capacitor placement. The method considers different load levels. Carpinelli [5] presents a method based on the sequential placement of capacitor units; process that cannot assure optimality of solution. Considers unbalance and several load levels.

Khalil [6] employs a binary-PSO to determine the placement of fixed and switched capacitors, while Ladjavardi [7] introduces another GA application with fuzzy-reasoning to manage as objectives the suitability of THD, voltage, and cost, while considers a single load state.

A discrete version of PSO is presented by Eajal [8] to minimize total cost while the THD complies with bounds. The method places fixed capacitors on unbalanced systems. Another PSO application is introduced by Taher [9] for fixed capacitors that uses penalty functions to manage constraints.

Mohkami [10] proposes a bacterial foraging (BF) oriented by PSO for placing fixed and switched capacitors. The analysis of sensitivities is used to select candidate nodes. Fuzzy multi-objectives are: cost, THD and voltage deviation.

Chang [11] presents a fuzzy logic and immune algorithm (IA) for placement and sizing of capacitors. The suitability of losses index, voltage, THD, and locations are modeled as fuzzy membership functions. The candidate locations are selected and the capacitors' sizes are calculated by the IA.

The non-dominated sorting genetic algorithm (NSGA-II) is used by Segura [12] to minimize the total cost and the quadratic sum of harmonics' voltages differences in respect to the base case. This contribution introduces the resonance index (RI) constraint to avoid the overstress of the capacitors. The methodology assumes the recommended current-distortion limits of IEEE Std. 519 [13] as the harmonics of the non-linear loads. Gonzalves [14] uses the extremal optimization (EO) heuristic to solve the capacitor placement taking into account resonance constraints. This method considers a single load state.

A hybrid honey bee colony algorithm is presented by Taher [15]. The method minimizes losses and unbalances while maintaining voltage and THD in an acceptable range. A penalty free GA is employed by Vuletic [16] for solving the capacitor placement with different load models. This approach considers fixed and switched capacitors.

The placement of fixed and switched capacitors with the NSGA-II is presented by Azevedo [17]. The formulation minimizes: cost, voltage deviation and THD. Also, Onaka [18] uses the NSGA-II for minimizing cost and voltage-deviations. Constraints of THD and IHD are evaluated, but a resonance index RI is employed to consider the capacitors' overstress limits after the optimization ends.

A multi-swarm particle swarm optimization (MSPSO) algorithm is proposed by Ayoubi [19]. A sensitivity analysis is applied to find candidate buses and the size and location of capacitors are optimized by MSPSO. It supports different load levels employing fixed and switched capacitors.

The Chu-Beasley GA is employed by Semensato [20] to the placement of capacitors in unbalanced circuits with one load state. Recently, Moghadam [21] has presented a new application of NSGA-II to minimize: cost, THD and voltage deviation. A single load state is considered.

Some of the contributions [1,10-12] use the losses sensitivity of nodes to obtain a reduced set of candidate nodes to locate the capacitors. This is a proper technique to simplify the optimization, but these locations set cannot be too small.

The consideration of several load levels with different cost and duration is fundamental to evaluate the capacitor placement effects on losses, voltages and other power quality constraints. However, some contributions [2,3,7-9,14,20, 21] analyze only one load state.

The IEEE Std. 519-2014 states recommended maximum values of THD and IHD to be complied. However, with the exception of a few contributions [11,16-18], only the THD constraints are considered.

The IEEE Std. 18-2012 [22] states the maximum permissible values for: rms voltage, peak voltage, current and reactive power of capacitor banks. Some references [12,18] try to avoid the overstress of the capacitors by introducing the resonance index, but only the references [16,17] fully addressed the required constraints.

This work presents a substantial improvement of the variables' inclusion and interchange algorithm (VIIA) for capacitors placement [23] that considers circuits with harmonic distortion. Several load states are considered and fixed and switched capacitors are employed in optimization. All the pertinent constraints of voltage magnitude, THD, IHD, and of overstress of capacitors are implemented. The here defined global harmonic-distortion index states the distance to the feasibility or the infeasibility of a solution with respect the harmonic distortion constraints. The inclusion in the sequential quadratic programming (SQP) sub-problem of an inequality linear constraint on this global harmonic-distortion index, allows the determining of solutions that comply with the harmonic distortion related constraints. A comparison of the solutions of various examples obtained by the presented method with the best solutions obtained by the Matlab's GA shows the effectiveness of this method.

2. Optimization problem

This work formulates the capacitor placement problem in distribution circuits with harmonic distortion as the selection, placement, and control in time of the set of capacitor banks that maximizes the saving in total annual cost.

The constraints of minimum and maximum voltage, as well as the pertinent constraints of power quality and of capacitors' overstress are considered.

2.1 Independent variables

The load's daily variation is represented by T states of load sorted in ascending order (normally: light, nominal and peak load). A capacitor that is switched-on in the t-load state will remain connected from this state up to the peak load state.

The capacitors can be placed in any of the N nodes of the circuit and can be switched-on in any of the T defined load states. Thus, there exist $L=N\cdot T$ possible locations for placing

the capacitors. The location of index *i* represents the node n_i and the switch-on time t_i of a single capacitor bank.

The independent variables of the problem are the vectors *x* and *u* of length (*M*x1) that represent respectively the sizes and locations of the capacitors. The elements of *u* are integers limited to the number of the possible locations, while the elements of *x* are the standard sizes of the capacitors placed in the *u* locations.

2.2 Objective function

The objective function of the optimization problem is the maximization of the total cost saving $F(x, u)$.

$$max\ F\ (x,u) = \sum_{t=1}^{T} c_t \Delta loss_t(x,u) - kc \sum_{i=1}^{M} x_i - kf \cdot M \quad (1)$$

Where c_t is the cost of losses in the load state *t* (\$/kW) and $\Delta loss_t(x, u)$ is the saving of losses in the *t* load state due to the installation of capacitors with sizes *x* on the *u* locations. The annual cost of capacitors is represented by the units cost *kc*(\$/kvar), and the fixed cost per capacitor bank *kf* (\$/bank). Besides, *M* is the number of capacitors.

2.3 Constraints

The voltage constraints assure that module of voltage *U* in every node and load state (*n,t*) will fulfill the desired lower and upper bounds *Umin* and *Umax*.

$$Umin \le |U(x,u)| \le Umax \quad (2)$$

Taken into account the recommendations of the IEEE Std. 519-2014, other voltage quality constraints are applied on the maximum distortion indexes *THD* and *IHD* in every node, load state and harmonic (*n,t,h*). These indices must comply with 5% and 3% limits respectively in medium voltage level.

$$max\ T\ HD = \underset{for\ every\ n,t}{max} \left\{ \sqrt{\sum_{h:>1} \left|U_{n,t,h}\right|^2} \Big/ \left|U_{n,t,1}\right| \right\} \le 0.05 \quad (3)$$

$$max\ I\ HD = \underset{for\ every\ n,t,h}{max} \left\{ \left|U_{n,t,h}\right| / \left|U_{n,t,1}\right| \right\} \le 0.03 \quad (4)$$

In addition, other constraints are stated to avoid the overstress of the capacitors by complying with recommended bounds by the IEEE Std. 18-2012. This standard state the limits of stress of the capacitors: the maximum peak voltage (*Ucpk*), the maximum rms voltage (*Uc*), the maximum current (*Ic*) and the maximum reactive power (*Qc*). The maximum of these indices for all capacitors must comply with:

$$max\ U\ cpk = \underset{for\ every\ i,t}{max} \left\{ \sum_h \left|Uc_{i,t,h}\right| / Ucnom_i \right\} \le 1.2 \quad (5)$$

$$max\ U\ c = \underset{for\ every\ i,t}{max} \left\{ \sqrt{\sum_h \left|Uc_{i,t,h}\right|^2} / Ucnom_i \right\} \le 1.1 \quad (6)$$

$$max\ I\ c = \underset{for\ every\ i,t}{max} \left\{ \sqrt{\sum_h \left|Ic_{i,t,h}\right|^2} / Icnom_i \right\} \le 1.35 \quad (7)$$

$$max\ Q\ c = \underset{for\ every\ i,t}{max} \left\{ \sum_h Qc_{i,t,h} / Qcnom_i \right\} \le 1.35 \quad (8)$$

Where sub-index *i* represents the capacitor bank.

In order to simplify the evaluation of the harmonic related constraints, a single normalized index of maximum distortion is proposed such that:

$$hmax = max\left\{ \frac{max\ THD}{0.05}, \frac{max\ IHD}{0.03}, \frac{max\ Ucpk}{1.2}, \frac{max\ Uc}{1.1}, \frac{max\ Ic}{1.35}, \frac{max\ Qc}{1.35} \right\} \le 1 \quad (9)$$

If the *hmax* index is equal or lower than unity, all the constraints of power quality and of capacitors' overstress are fulfilled.

2.5 Problem formulation

Finally, the optimization problem can be stated as the determination of the number of capacitors *M*, the *u*-locations (node and switched-on time) and the *x*-sizes that solves the problem represented by:

$$max\ F\ (x,u) = \sum_{t=1}^{T} c_t \Delta loss_t(x,u) - kc \sum_{i=1}^{M} x_i - kf \cdot M$$

subjet to

$$Umin \le |U(x,u)| \le Umax$$
$$hmax(x,u) \le 1$$
$$x \ge 0 \quad (10)$$

3. Sequential quadratic programming approach

For a given number of capacitors and *u*-locations, the capacitors' optimal *x*-sizes are obtained by applying the Sequential Quadratic Programming (SQP) method. This method solves a nonlinear optimization problem by solving a sequence of optimization sub-problems, each of which is formed by a quadratic objective function subject to a linearization of the constraints of the original problem.

3.1 Sub-problem's quadratic objective function

The quadratic sub-problem's objective function is obtained from (1) by considering a linear approximation for the variations of voltages with respect to the Δx-capacitors' sizes variations.

As losses at harmonic frequencies are negligible with respect to the losses at fundamental frequency, only the fundamental frequency losses saving is considered in the presented model. The fundamental frequency power losses saving at the *t* load state is the difference of the losses before and after the capacitors placement.

$$\Delta loss_t(x,u) = U_t^* G U_t - (U_t + \Delta U_t)^* G (U_t + \Delta U_t) \quad (11)$$

Where U_t and ΔU_t are column vectors (*Nx1*) that represent the fundamental frequency voltages without capacitors and their variation by the effect of the capacitors at the load state *t*. Besides, *G* is the fundamental frequency conductance

matrix of the network. The matricial operation z^* denotes the transposed conjugate of the matrix z.

The variation of fundamental-frequency voltages ΔU_t due to variations of the capacitors of sizes x can be approximate by the linear relation:

$$\Delta U_t = J_t \cdot \Delta x \tag{12}$$

The elements of the matrix J_t of size (NxM) are derivatives of the voltage at load state t in node n respect the susceptance of the capacitor installed in node m.

$$J_{n,m,t} = \frac{\partial U_{n,t}}{\partial x_m} = \frac{\partial U_{n,t}}{\partial Q_{m,t}} \left|U_{m,t}\right|^2 \tag{13}$$

The derivatives of voltage in the node n with respect to the variation of the reactive power in the node m are extracted from the inverse of the Jacobian matrix of the Newton-Raphson load flow.

Substituting (12) in (11) is obtained an approximated quadratic model for the reduction of losses at the state t.

$$\begin{aligned} \Delta loss_t(x) &= -x^T(2 \cdot re\{J_t{}^* G \cdot U_t\} + re\{J_t{}^* G \cdot J_t\}x) \\ &= x^T(2b_t - D_t x) \end{aligned} \tag{14}$$

Integrating the saving of losses in all load states, the quadratic objective function of the sub-problem can be approximated by:

$$\Delta F(x) \approx \Delta x^T(2d(x) - A(x) \cdot \Delta x) \tag{15}$$

The elements of vector d are determined for the capacitor i placed in the node n_i and switched-on in state t_i, as:

$$d_i = \sum_{t=t_i}^{T} b_{n_i,t} c_t - \frac{1}{2} kc \tag{16}$$

The elements of A-matrix are determined by the interaction of the capacitor i and the capacitor j (which is placed in the node n_j and switched-on in state t_j) as:

$$A_{i,j} = \sum_{t=max(t_i,t_j)}^{T} D_{n_i,n_j,t} c_t \tag{17}$$

3.2 Sub-problem's linear constraints

Although the harmonic voltages can affect the rms voltage magnitude on the nodes, normally this influence is very reduced if there are no resonances in the circuit. In order to simplify the representation of the voltage constraints, only the fundamental frequency voltage will be considered.

Substituting (12) in (2), the maximum and minimum voltage constraints at load state t can be expressed by:

$$Umin \leq |U_t| + W_t \cdot \Delta x \leq Umax \tag{18}$$

Where the elements of the matrix W_t are determined by:

$$W_{n,m,t} = \frac{\partial |U_{n,t}|}{\partial x_m} = re\{U_{n,t}{}^* J_{n,m,t}\} / \left|U_{n,t}\right| \tag{19}$$

In general, if U represents the vector of voltages in every nodes and load states, the minimum and maximum voltage constraints can be expressed as:

$$-Jmin \cdot \Delta x \leq -bmin = -(Umin - |U|) \tag{20}$$

$$+Jmax \cdot \Delta x \leq +bmax = +(Umax - |U|) \tag{21}$$

In spite of the nonlinearities related with the harmonics penetration in a network with capacitors installed, in this work is developed a linear approximation of the previously defined harmonic distortion *hmax*-index (9). This approximation is based on determining the variations produced in *hmax* when each variable (capacitor) of the solution is increased one standard unit while the others remain the same.

If the vector x represents the sizes of the installed capacitors, a variation Δx that makes that the solution complies with the harmonic distortion bounds must be limited by the linear constraint:

$$Jh \cdot \Delta x \leq bh = 1 - hmax(x) \tag{22}$$

Each element Jh_i is the ratio of the variation of the harmonic distortion index $\Delta hmax(x)$ with respect the variation Δx_i of the variable x_i:

$$Jh_i = (hmax(x + \Delta x_i) - hmax(x))/\Delta x_i \tag{23}$$

The obtaining of each Jh_i element requires the use of the harmonics penetration function to calculate the harmonics distortion index when only the variable x_i is incremented in one standard unit.

3.3 Sub-problem's representation

The quadratic programming model of this sub-problem is represented by:

$$\begin{aligned} &max\, \Delta F(\Delta x) = \Delta x^T(2 \cdot d(x) - A(x) \cdot x\Delta) \\ &\text{subject to} \\ &\quad -Jmin(x)\Delta x \leq bmin(x) \\ &\quad Jmax(x)\Delta x \leq bmax(x) \\ &\quad Jh(x)\Delta x \leq bh(x) \\ &\quad x + \Delta x \geq 0 \end{aligned} \tag{24}$$

The SQP method solves the problem (10) by the successive determination of the best feasible variation Δx that solves the quadratic sub-problem (24). The first iteration begins with $x = 0$ (without capacitors) and next iterations increase x by $x + \Delta x$. Only a few iterations are needed to obtain convergence of x.

4. Algorithm of optimization

The determination of the x-sizes of M-capacitors in the given u-locations is solved by the SQP method. However, the locations (switched-on time and placement) and the number of capacitors must be determined by searching within the possible sets of variables (locations) that can integrate a solution.

The VIIA is composed by two consecutive phases: 1) the search of solutions; and 2) the selection of optimal solution.

In the search phase, the algorithm examines a reduced subset of the possible sets of variables (solutions). The *x*-sizes corresponding to a given *u*-locations are obtained by solving the approximate quadratic sub-problem (24) of the base case by the function SQP1, which implements only the first iteration of the SQP method.

The transit from one set of variables (solution) to another is based on their relative merit, which is measured by the penalized objective function value $Fp(x)$. The best 500 solutions examined in this search phase are stored in the best solutions list.

Once the search phase is finished, the list of best solutions is sorted in descending order of the non-penalized objective function value $F(x)$ and in ascending order of the harmonics distortion index $hmax(x)$.

These 500 solutions have been obtained by only the first iteration of the SQP method. Thus, they are approximate solutions that have not been tested by the fundamental frequency load flow (FFLF) and the harmonics penetration function (HPF). Then, each solution of the list is improved by the function SQP2, which implements the final iterations of the SQP method, until a convergence of the capacitors sizes is achieved. The best of the obtained solutions is selected as optimal.

4.1 Description of the search algorithm

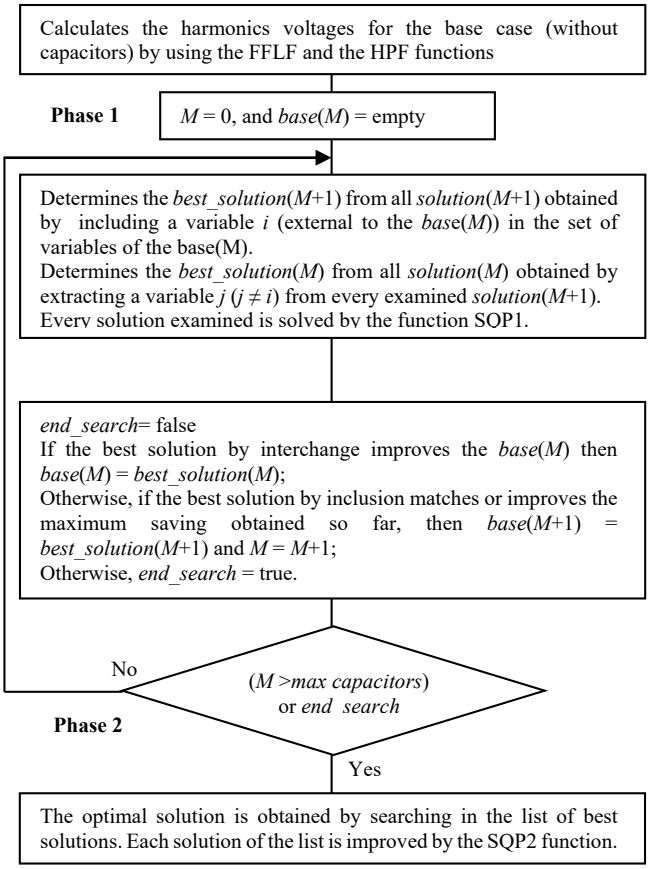
The search algorithm begins from the empty solution $base(0)$ (number of capacitors $M = 0$). The solution grows in number of variables (capacitors) from the $base(0)$ solution up to the solution with the maximum $Fp(x)$. In each step, departing from the $base(M)$ of M capacitors, a new solution is obtained by adding a new variable (location) to the $base(M)$ or by interchanging a variable of the $base(M)$ solution with a variable external to this solution. This algorithm is described by the Flowchart 1.

If the number of possible variables (locations) is L. One iteration of the presented search algorithm departing from the $base(M)$, requires the evaluation of $(L - M)$ solutions by inclusion of a variable and of $(L - M)M$ solutions by interchange of variables. Thus, when the number of possible variables is high or the number of capacitors grows, the number of solutions to be evaluated is high.

The experience of use of the presented algorithm has proven that results are good enough if just a sub-set of the variables of a $solution(M+1)$ is tested to obtain solutions of M variables by interchange.

In that way, the variables in a $solution(M+1)$ are sorted in ascending order of their importance (size of the capacitors) and only the first out ($out < M$) variables are tested for extraction. In the presented implementation of the algorithm, $out = 1$ for solutions with low harmonics distortion ($hmax(x) \leq 0.95$) and $out = 4$ otherwise.

On the other hand, the number of possible variables L can be reduced by preselecting a subset of nodes or a subset of load states. In the presented implementation, only 40 nodes are preselected for capacitor placement in each load state. The selection is based on the saving obtained by the capacitor placed on node i and switched-on at t-load state, that is, $F_{i,t} = d_{i,t}^2/A_{i,i,t}$. In that way, the maximum number of variables $L \leq 40T$ is independent of the circuit's size



Flowchart 1.
Source: The author.

The presented algorithm, including the FFLF for radial distribution systems, as well as the HPF, have been implemented in Matlab R2017a.

4.2 Algorithms of functions SQP1 and SQP2

For a given set of variables, the function SQP1 calculates an approximated solution x for the problem (10) by solving the sub-problem (24) (first iteration of the SQP method). The calculated objective function is used by the search algorithm to rank the solution.

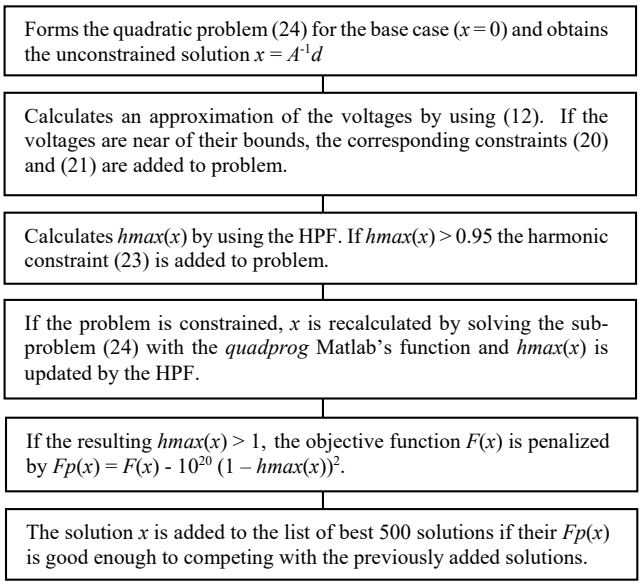
The algorithm of the function SQP1 is described by the Flowchart 2.

On the other hand, the function SQP2 improves the approximate solution x by repeating the final iterations of the SQP method until convergence is found. This function employs a fundamental frequency load flow and a harmonics penetration function to determine exactly the objective function value $F(x)$, the voltages of all frequencies and the harmonics distortion index $hmax(x)$.

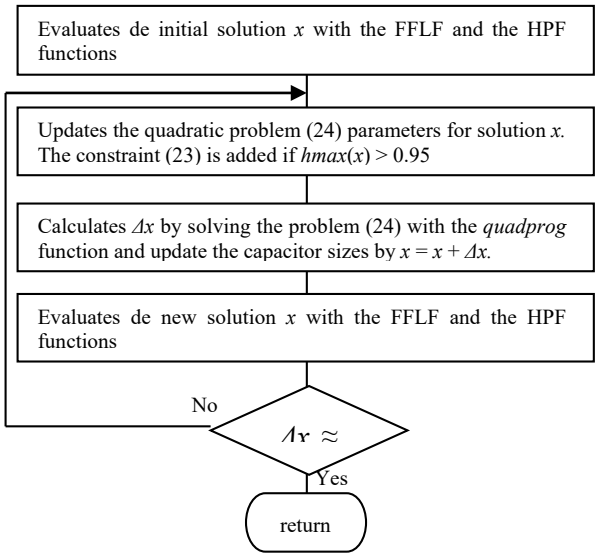
The Flowchart 3 describes the algorithm of function SQP2.

5. Examples of application

In order to test the presented methodology, four known radial distribution systems of: 33, 34, 69 and 85 nodes are used. The data of the 12.66 kV's circuits of 33 and 69 nodes



Flowchart 2.
Source: The author.



Flowchart 3.
Source: The author.

are presented in the reference [24], while the data of the 11 kV's circuits of 34 and 85 nodes are reproduced in the reference [25].

In all the following examples, the circuit operates in three load states of 0.5, 1 and 1.6 times the nominal load, with duration of 2000, 5260 and 1500 hours/year respectively. The losses cost is c_t = \$0.06/kWh in all load states and the annual cost of capacitors is calculated with kc = \$3/kvar and kf = \$1000/bank. A maximum of 15 capacitor banks composed of standard units of 150 kvar can be installed.

All circuits are supplied by a voltage source with 250 MVA of short circuit power with ratio X/R = 10. The source voltage is nominal with certain harmonics content represented by the harmonic spectrum of Table 1.

Table 1.
Harmonic spectrums for examples

Order h	Nonlinear load current I_h(%)	Angle(deg)	Voltage source U_h(%)	Angle(deg)
1	100.00	-13.80	100.00	30.30
5	19.54	109.60	0.81	1.40
7	10.25	85.20	0.59	-21.20
11	5.14	-153.00	0.45	100.30
13	3.40	-180.00	0.35	72.40
17	1.00	-64.40	0.13	-174.40
19	0.60	-98.90	0.09	149.70

Source: The author.

Table 2.
Solutions for example of the circuit of 33 nodes

		Case 33-1a		Case 33-1b	
Solution	Base case	VIIA	GA	VIIA	GA
Saving(\$)	0.00	18024.19	15705.43	20318.10	20758.54
T.Cost(\$)	127342.79	109318.60	111637.36	107024.69	106584.25
Losses(\$)	127342.79	96418.60	98287.36	93674.69	90884.25
C.Cost(\$)	0.00	12900.00	13350.00	13350.00	15700.00
Cap(kvar)	0.00	3300.00	3450.00	3450.00	3900.00
Time(s)		34.50	198.73	37.14	331.83

	t	Bus		Bus		Bus		Bus		Bus	
Losses (kW)	1		48.76		47.51		48.76		46.94		43.22
	2		211.86		167.92		175.10		163.52		157.51
	3		606.98		419.12		413.05		404.84		399.86
Umax (%)	1	1	100.01	1	100.00	1	100.01	1	100.00	1	100.00
	2	1	100.01	1	100.00	1	100.00	1	100.01	1	100.00
	3	1	100.01	1	100.01	1	100.01	1	100.01	1	100.01
Umin (%)	1	18	95.40	18	96.32	18	95.40	33	96.64	18	97.16
	2	18	90.39	30	95.40	33	92.73	18	94.33	18	92.60
	3	18	83.64	18	90.06	18	90.01	18	88.52	33	89.39
max THD(%)	1	30	1.53	31	1.90	30	1.53	13	1.66	13	3.03
	2	30	3.02	31	3.15	31	2.53	13	3.08	30	4.07
	3	33	5.39	31	3.08	16	3.24	31	3.10	16	4.20
max IHD(%)	1	30	(11^{th})1.05	31	(5^{th})1.69	30	(11^{th})1.05	13	(7^{th})1.46	13	(7^{th})2.93
	2	30	(11^{th})1.74	16	(5^{th})2.78	31	(5^{th})1.95	16	(5^{th})2.72	31	(5^{th})2.78
	3	33	(5^{th})3.24	18	(5^{th})2.99	33	(5^{th})2.78	31	(5^{th})2.86	31	(5^{th})2.97
Cap. (kvar)	1			31	1050		12		750	7	1350
	2			14	1050	8	1200	30	1800	29	450
	3			31	1200	16	450	30	900	14	450
	3					33	1800			31	1650

Source: The author.

All loads are modeled as constant active and reactive power at fundamental frequency, while at harmonic frequencies; the linear load is modeled by the series RL circuit [26] and the nonlinear load current is represented by the harmonics' spectrum of Table 1.

Two types of capacitors placement problems are solved in the examples: a) a voltage-constrained problem that assures a minimum voltage of 0.9 pu for solutions; and b) a voltage-unconstrained problem. In all cases, the solutions proposed by the presented search algorithm are compared with the best solutions determined by three consecutive runs of the genetic algorithm implemented in the *ga* function of Matlab R2017a.

To obtain good solutions for the examples with the GA, a large population of 1000 individuals and a maximum of 300 generations was used. Other data of the GA's configuration are presented in appendix. The results of the GA in all presented cases are the best solutions found in three consecutive runs of the algorithm.

All examples were solved in a Intel(R) Pentium(R) CPU P6100 @ 2.00Ghz -2.00Ghz and 8.00 GB RAM. In that way the computation time of all runs can be compared among them.

5.1 Minimum cost optimization in the circuit of 33 nodes

The circuit of 33 nodes have a total load of 3715 kW and 2300 kvar. In the example, all the load in nodes 24, 25 and 30 is nonlinear, which represents the 28% of the total active load and the 43% of the total reactive load. The results of the optimization of this example are presented in Table 2.

The base case (without capacitors) does not comply with the IEEE-519 recommendations because the maximum *THD* = 5.39% and *IHD* = 3.24% are outside the limits in the peak load status.

The first case analyzed (33-1a) includes the constraint of minimum-voltage of 0.9 pu. The proposed solution improves the GA's solution in 14.8% by using the 95.7% of capacitor units. The presented algorithm obtains the solution in only the 17.4% of the GA's computation time.

In the second case (33-1b) (voltage unconstrained), the proposed solution is inferior in 2.1% respect the GA's solution. The proposed solution uses the 88% of capacitors' units and is obtained in just an 11.2% of the GA's computation time.

5.2 Minimum cost optimization in the circuit of 34 nodes

The circuit of 34 nodes have a total load of 4636.5 kW and 2873.5 kvar. As the minimum voltage of this circuit is greater than 0.9 pu, there is no difference between the constrained voltage solution and the unconstrained voltage solutions. Thus, the solutions of two different voltage-unconstrained examples are presented.

Table 3.
Solutions for example 1 of the circuit of 34 nodes

			Case 34-1b				
Solution			Base case		VIIA		GA
Saving($)			0.00		21309.80		21733.85
T.Cost($)			131088.38		109778.58		109354.53
Losses($)			131088.38		100928.58		100054.53
C.Cost($)			0.00		8850.00		9300.00
C.(kvar)			0.00		1950.00		2100.00
Time(s)					22.43		344.42
	t	**Bus**		**Bus**		**Bus**	
Losses (kW)	1		53.16		41.30		41.57
	2		222.42		166.03		164.12
	3		605.69		484.15		480.78
Umax (%)	1	1	100.01	1	100.03	1	100.01
	2	1	100.01	1	100.02	1	100.02
	3	1	100.01	1	100.02	1	100.02
Umin (%)	1	27	97.17	27	97.51	27	97.70
	2	27	94.18	27	94.98	27	94.95
	3	27	90.36	27	91.19	27	91.16
max THD(%)	1	27	1.36	27	3.74	27	2.85
	2	27	1.67	27	3.03	27	3.09
	3	27	2.16	27	3.65	27	3.68
max IHD(%)	1	27	(5^{th})0.81	27	(11^{th})2.65	27	(11^{th})2.08
	2	27	(7^{th})0.91	27	(7^{th})2.42	27	(7^{th})2.54
	3	27	(7^{th})1.13	27	(7^{th})2.88	27	(7^{th})2.99
Cap. (kvar)	1			10	600	9	750
	1			21	450	24	750
	2			26	900	21	600

Source: The author.

Table 4.
Solutions for example 2 of the circuit of 34 nodes

			Case 34-2b				
Solution			Base case		VIIA		GA
Saving($)			0.00		20563.00		20634.51
T.Cost($)			131271.56		110708.56		110637.06
Losses($)			131271.56		103308.56		103237.06
C.Cost($)			0.00		7400.00		7400.00
C.(kvar)			0.00		1800.00		1800.00
Time(s)					18.47		334.25
	t	**Bus**		**Bus**		**Bus**	
Losses (kW)	1		53.29		44.18		45.43
	2		222.75		169.09		168.96
	3		606.40		496.02		494.02
Umax (%)	1	1	100.01	1	100.02	1	100.01
	2	1	100.01	1	100.02	1	100.02
	3	1	100.01	1	100.02	1	100.02
Umin (%)	1	27	97.17	27	97.68	27	97.71
	2	27	94.19	27	94.83	27	94.88
	3	27	90.37	27	91.05	27	91.10
max THD(%)	1	27	1.46	27	3.52	27	3.11
	2	27	1.92	27	3.20	27	3.22
	3	27	2.62	27	4.11	27	4.12
max IHD(%)	1	27	(5^{th})0.82	27	(11^{th})2.92	27	(11^{th})2.42
	2	27	(7^{th})1.02	27	(7^{th})2.31	27	(7^{th})2.38
	3	27	(7^{th})1.33	27	(7^{th})2.89	27	(7^{th})2.97
Cap. (kvar)	1			23	1050	24	1050
	1						
	2			10	750	10	750

Source: The author.

In the first example (34-1b) with results shown in Table 3, the 50% of load in nodes 17, 21 and 26 is nonlinear. This means the 7% of total load. However, the base case complies with the power quality constraints. The proposed solution is 2% inferior respect to the GA's solution. However, this solution is obtained in only the 6.5% of the GA's computation time. Three banks are proposed with the 92.9% of the capacitor's units used by GA's solution.

In the second example (34-2b) with results shown in Table 4, the 20% of load in nodes 17-26 is nonlinear. Thus, the 10% of total load is nonlinear. Although the harmonic distortion is incremented, the base case complies with the IEEE-519's distortion limits. The proposed solution is only 0.35% inferior to the GA's solution but is obtained in just a 5.5% of the computation time employed by the GA.

5.3 Minimum cost optimization in the circuit of 69 nodes

The circuit of 69 nodes have a total load of 3801.39 kW and 2693.6 kvar. Two different examples are analyzed with concentrated and distributed nonlinear loads.

In the first example (1), which results shown in Table 5, the 50% of load in nodes 49, 50 and 61 is nonlinear, which represents the 26% of total load.

This example complies with the IEEE-519's harmonic limits, but the maximum THD reaches the 87.7% of their bound in the peak load state.

The solution proposed for the constrained case (69-1a) improves the GA's solution in 3.1%, uses the 103.7% of the total capacitor units and is obtained in only the 11% of the GA's computation time. In the second case (69-1b), the proposed solution is superior in 3.1% respect the GA's

Table 5.
Solutions for example 1 of the circuit of 69 nodes

		Case 69-1a			Case 69-1b	
Solution		Base case	VIIA	GA	VIIA	GA
Saving($)		0.00	26607.48	25809.27	29333.72	28457.60
T.Cost($)		136130.97	109523.49	110321.70	106797.25	107673.37
Losses($)		136130.97	92923.49	95171.70	90097.25	92973.70
C.Cost($)		0.00	16600.00	15150.00	16700.00	14700.00
Cap.(kvar)		0.00	4200.00	4050.00	3900.00	3900.00
Time(s)			34.15	311.34	77.95	356.62
	t	Bus	Bus	Bus	Bus	Bus
Losses (kW)	1	51.39	37.10	47.50	34.21	47.18
	2	225.19	151.80	151.85	150.43	152.49
	3	654.39	450.70	461.65	427.95	435.40
Umax (%)	1	1 100.01	1 100.00	1 100.01	1 100.01	1 100.02
	2	1 100.01	1 100.00	1 100.00	1 100.00	1 100.00
	3	1 100.01	1 100.01	1 100.01	1 100.01	1 100.01
Umin (%)	1	65 95.68	61 96.67	65 95.84	65 96.64	65 95.91
	2	65 90.95	65 93.41	65 93.24	65 93.10	65 93.29
	3	65 84.53	65 90.05	61 90.14	65 89.44	65 89.50
max THD(%)	1	65 1.33	65 2.31	27 2.64	65 2.73	27 3.48
	2	65 2.43	65 3.40	65 3.36	65 3.68	65 3.33
	3	65 4.39	65 2.65	65 2.71	65 3.19	65 3.20
max IHD(%)	1	65 (11th)0.93	65 (11th)1.63	27 (13th)1.97	65 (11th)2.16	27 (13th)2.88
	2	65 (11th)1.49	65 (7th)2.36	65 (7th)2.42	65 (7th)2.96	65 (7th)2.36
	3	65 (5th)2.43	65 (5th)2.46	65 (5th)2.48	65 (5th)2.99	65 (5th)2.99
Cap. (kvar)	1	64	600	12 450	12 300	10 600
	1			61	600	
	2	17	450	61 1500	17 300	61 1500
	2	61	900	61	750	
	3	61	2250	64 2100	62 1950	63 1800

Source: The author.

Table 6.
Solutions for example 2 of the circuit of 69 nodes

		Case 69-2a			Case 69-2b	
Solution		Base case	VIIA	GA	VIIA	GA
Saving($)		0.00	24435.70	23004.01	25514.95	26505.23
T.Cost($)		136199.23	111763.53	113195.22	110684.28	109694.00
Losses($)		136199.23	97063.53	95245.22	94084.28	94544.00
C.Cost($)		0.00	14700.00	17950.00	16600.00	15150.00
Cap.(kvar)		0.00	3900.00	4650.00	4200.00	4050.00
Time(s)			35.33	460.55	80.57	428.61
	t	Bus	Bus	Bus	Bus	Bus
Losses (kW)	1	51.36	38.10	36.18	37.16	50.54
	2	225.28	160.27	158.60	154.13	153.49
	3	654.87	465.67	453.89	455.37	444.85
Umax (%)	1	1 100.01	1 100.00	1 100.00	1 100.01	1 100.01
	2	1 100.01	1 100.00	1 100.00	1 100.00	1 100.00
	3	1 100.01	1 100.00	1 100.01	1 100.01	1 100.01
Umin (%)	1	65 95.68	61 96.88	65 96.80	65 97.06	65 95.82
	2	65 90.95	65 93.39	65 93.17	65 93.26	65 93.26
	3	65 84.55	65 90.02	65 90.00	65 89.91	65 89.76
max THD(%)	1	65 1.43	65 2.47	65 2.37	65 2.83	27 3.30
	2	65 2.74	65 3.93	65 4.03	65 3.91	65 3.89
	3	65 4.98	64 3.14	63 3.17	61 3.01	62 3.19
max IHD(%)	1	65 (11th)0.99	65 (7th)2.19	65 (7th)1.88	65 (7th)2.63	27 (11th)2.98
	2	65 (11th)1.62	65 (5th)2.81	65 (7th)2.86	65 (7th)2.75	65 (5th)2.77
	3	65 (5th)2.85	64 (5th)2.93	63 (5th)2.95	61 (5th)2.82	62 (5th)3.00
Cap. (kvar)	1	64	750	63 750	18 300	21 450
	1			61	900	
	2	60	900	61 750	59 750	61 1500
	3	61	2250	54 1200	61 2250	62 2100
	3			61 1950		

Source: The author.

solution and is obtained in the 21.8% of the GA's computation time.

In the second example (2), which results offered in Table 6, the 50% of load in nodes 49, 50 and 61, and the 10% of load in the rest of nodes is nonlinear, which totalizes the 31% of total load. This base case complies with the IEEE-519's recommendations, but the maximum THD almost reach the IEEE-519's recommended limit of 5% in the peak load status.

The first case analyzed (69-2a) includes the constraint of minimum voltage of 0.9 pu. The proposed solution improves the GA's solution in 6.2% by using the 83.9% of capacitor units in the GA's solution. The presented algorithm obtains the solution in only the 7.7% of the GA's computation time.

In the second case (69-2b), the proposed solution is inferior in 3.7% and uses the 103.7% of capacitor units with respect the GA's solution. The solution is obtained in the 18.8% of the GA's computation time.

5.4 Minimum cost optimization in the circuit of 85 nodes

The circuit of 85 nodes have a total load of 2569.28 kW and 2621.19 kvar. Two different examples with harmonic distortion indices above the IEEE-519's recommended limits are analyzed.

In the first example (1), which results shown in Table 7, the 25% of load in all nodes is nonlinear. The maximum distortion indices in peak load state THD = 6.08% and IHD = 3.6% are the 121.6% and the 119.8% respect to their respective limits in the standard IEEE-519.

Table 7.
Solutions for example 1 of the circuit of 85 nodes

		Case 85-1a			Case 85-1b	
Solution		Base case	VIIA	GA	VIIA	GA
Saving($)		0.00	77659.25	75390.44	87540.50	86676.58
T.Cost($)		196413.25	118754.00	121022.81	108872.75	109736.67
Losses($)		196413.25	96654.00	93922.81	91172.75	92036.67
C.Cost($)		0.00	22100.00	27100.00	17700.00	17700.00
Cap.(kvar)		0.00	5700.00	5700.00	3900.00	3900.00
Time(s)			71.04	989.32	32.45	523.70
	t	Bus	Bus	Bus	Bus	Bus
Losses (kW)	1	70.06	47.04	44.34	41.23	43.41
	2	316.59	155.62	151.34	151.43	153.23
	3	978.78	465.49	453.78	427.03	427.41
Umax (%)	1	1 100.01	1 100.00	1 100.01	1 100.00	1 100.00
	2	1 100.01	1 100.01	1 100.01	1 100.01	1 100.01
	3	1 100.01	1 100.00	1 100.01	1 100.01	1 100.01
Umin (%)	1	54 93.98	54 95.94	54 95.43	54 96.08	54 96.37
	2	54 87.18	54 91.96	54 92.47	54 92.49	54 92.49
	3	54 77.37	47 90.01	47 90.04	54 86.08	54 86.04
max THD(%)	1	54 1.52	64 1.41	54 2.75	84 2.09	12 1.53
	2	54 3.11	32 3.02	34 2.76	48 2.82	55 2.83
	3	54 6.08	52 1.80	53 1.85	48 2.93	55 2.92
max IHD(%)	1	54 (11th)1.06	76 (7th)1.19	54 (7th)2.44	84 (7th)1.97	84 (7th)1.31
	2	54 (11th)1.80	32 (5th)2.87	34 (5th)2.55	48 (5th)2.65	55 (5th)2.65
	3	54 (5th)3.60	52 (5th)1.59	53 (5th)1.70	48 (5th)2.71	55 (5th)2.71
Cap. (kvar)	1	11	600	23 300	11 600	12 600
	1	64	750	29 600	28 600	28 750
	2	32	1050	10 750	48 600	55 450
	2		34	600	67 750	72 750
	2	64	600			
	3	9	2250	13 450	33 750	40 750
	3	52	1050	25 600	60 600	61 600
	3		48	600		
	3		53	600		
	3		68	600		

Source: The author.

The solution proposed for the voltage-constrained case (85-1a) improves the GA's solution in 3% and uses only the 81.5% of the total capacitor units in GA's solution. The presented algorithm obtains the solution in only the 7.2% of the GA's computation time.

In the second case (85-1b), the proposed solution is superior in 1% respect the GA's solution, uses the same amount of capacitors' units and is obtained in the 6.2% of the GA's computation time.

In the second example (2), which results offered in Table 8, the 30% of load in all nodes is nonlinear. This base case presents a heavy harmonic distortion with maximum indices THD = 7.4% and IHD = 4.52%, which means the 148% and the 150.8% of the limits recommended by the IEEE-519 standard.

The first case (85-2a) includes the constraint of minimum voltage of 0.9 pu. The proposed solution reaches the 99.4% of saving of the GA's solution by using the same amount of capacitor units. The presented method employs the 35.6% of the GA's computation time.

In the second case (85-2b), the proposed solution increases in 0.47% the saving of the GA's solution using only the 97.2% of the capacitor units in the GA's solution. The solution is obtained in the 7.5% of the GA's computation time.

Table 8.
Solutions for example 2 of the circuit of 85 nodes

		Case 85-2a			Case 85-2b	
Solution		Base case	VIIA	GA	VIIA	GA
Saving($)		0.00	74979.54	75440.87	86035.82	85636.00
T.Cost($)		196666.69	121687.14	121225.82	110630.87	111030.69
Losses($)		196666.69	99037.14	95575.82	91580.87	91430.69
C.Cost($)		0.00	22650.00	25650.00	19050.00	19600.00
Cap.(kvar)		0.00	5550.00	5550.00	4350.00	4200.00
Time(s)			238.93	670.90	77.08	1028.12
	t	Bus	Bus	Bus	Bus	Bus
Losses (kW)	1	70.12	40.20	38.91	40.05	41.53
	2	316.98	158.39	155.83	153.95	153.74
	3	980.14	491.41	463.64	421.64	421.39
Umax (%)	1	1 100.01	1 100.00	1 100.00	1 100.00	1 100.00
	2	1 100.01	1 100.01	1 100.01	1 100.01	1 100.01
	3	1 100.01	1 100.00	1 100.01	1 100.01	1 100.01
Umin (%)	1	54 93.99	54 96.10	54 96.18	54 96.03	54 96.77
	2	54 87.20	54 92.92	54 92.66	54 92.55	54 92.91
	3	54 77.44	47 90.03	55 90.02	54 86.74	54 86.33
max THD(%)	1	54 1.75	76 2.42	54 3.10	84 2.50	56 1.98
	2	54 3.76	34 2.89	34 3.04	35 3.16	56 3.15
	3	54 7.40	52 2.00	53 2.16	40 2.85	56 3.13
max IHD(%)	1	54 (11th)1.18	76 (7th)2.21	54 (7th)2.84	84 (7th)2.32	56 (7th)1.41
	2	54 (11th)2.07	34 (5th)2.73	34 (5th)2.88	35 (5th)2.99	56 (5th)2.96
	3	54 (5th)4.52	52 (5th)1.91	53 (5th)2.04	40 (5th)2.65	56 (5th)2.92
Cap. (kvar)	1	27	750	34 450	11 600	12 450
	1	64	450	60 600	27 600	56 450
	1					68 450
	2	11	900	13 450	35 600	29 750
	2	34	750	32 450	67 900	57 750
	2		57	900		
	3	52	1200	33 750	40 900	40 600
	3	67	1500	53 750	60 750	77 750
	3		72	900		
	3		81	300		

Source: The author.

6. Conclusion

The presented method optimizes the capacitors placement on distribution circuits contaminated by the presence of nonlinear loads.

Several load states with different magnitude and duration are considered, which allows the simultaneous determination of the number, size, placement and time-control of fixed and switched capacitors. All loads of the circuit must follow the same daily pattern of variation.

This method does not use sensitivity factors to preselect the locations to place the capacitors, instead selects a large set of candidate locations where the capacitors can be placed. That set is sufficient to allow that the search algorithm examine a great number of possible locations.

Different harmonic spectrums can be selected for representing the systems power source voltage and each of the nonlinear loads currents in the circuit.

The formulation guarantees the obtaining of feasible solutions (composed by standard units) that comply with the voltage's power quality constraints and with the capacitors overstress constraints.

The good results obtained in the solving of the presented examples is the best proof of the effectiveness of the constraint (22) in controlling the harmonic distortion.

The experience of use of this methodology shows that even some severe distortion cases can be solved. More difficult cases that cannot be solved with this method normally requires passive filters to compensate the reactive power and mitigate harmonic problems.

Although the modifications made for consider the harmonic distortion, augment the calculating burden of the method, the variables' inclusion and interchange algorithm is still efficient in the search of solutions.

7. Appendix

To solve the maximization problem expressed in (10), the genetic algorithm minimizes a fitness function expressed by:

$$fitness(chromosome) = -F(x,u) + \mu \cdot \sum_{c_i>1}(1-c_i)^2 \quad \text{(A.1)}$$

Where the elements of c, are maximum-ratios of the constrained parameters with respect their bounds. The penalty factor $\mu = 10^{20}$.

$$c = max\left\{\frac{max|U|}{Umax}, \frac{Umin}{min|U|}, \frac{max\,T\,HD}{0.05}, \frac{max\,I\,HD}{0.03}, \frac{max\,U\,cpk}{1.2}, \frac{max\,U\,c}{1.1}, \frac{max\,I\,c}{1.35}, \frac{max\,Q\,c}{1.35}\right\} \quad \text{(A.2)}$$

All the needed parameters are calculated from data in chromosome by the fundamental frequency load flow and the harmonic penetration function.

Instead of using directly the u-locations and the x-sizes of capacitors as independent variables, is used a chromosome which structure is represented in Table A.1.

The array of weights q and the total reactive compensation *Qtotal* are the parameters used for determining the sizes of the capacitors by:

Table A.1.
Structure of the chromosome

Elements	Variables	Min	Max	Description
1 ... nvar	$u_1 ... u_{nvar}$	1	*N·T*	Locations
nvar+1 ... 2nvar	$q_1 ... q_{nvar}$	0	1	Distribution factors
2nvar + 1	*Qtotal*	*unit*	1.2 *Qmax*	Total compensation
2nvar + 2	*M*	1	*nvar*	Number of capacitors

Source: The author.

$$x_i = (q_i/\sum_k q_k)Qtotal \quad \text{(A.3)}$$

This representation avoids the obtaining of a solution with over-compensation, because *Qtotal* is limited to 1.2 times the maximum total reactive load of the circuit. Besides, the *M* parameter is the number of selected capacitor banks.

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