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Verification of a Fabless Device Model Using TCAD Tools: from Bipolar Transistor Formation to I-V Characteristics Extraction

Verificación de un modelo de dispositivo sin defectos utilizando herramientas TCAD: desde la formación de transistores bipolares hasta la extracción de características I-V

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ABSTRACT

This paper describes the analysis of processes used in micro- and nano-electronic device manufacturing. It also presents an exemplary and novel laboratory exercise in which an epitaxial planar *n* + *pn* bipolar transistor with junction isolation is illustrated and analyzed step-by-step. Only seven photolithography steps are used to obtain this bipolar transistor structure: for buried layer formation, for junction transistor isolation and collectors regions formation, for base region formation, for emitter and collector *n*+ region formation, for contact windows, for first aluminum metallization, and, finally, for passivation. Silvaco TCAD software tools are used to implement all of these manufacturing processes and to simulate the resulting I-V characteristics of all presented semiconductor structures. This type of laboratory work provides students with basic knowledge and a consistent understanding of bipolar transistor manufacturing, as well as facilitating theoretical understanding, analysis, and simulation of various semiconductor manufacturing processes without the need for costly and lengthy technological manufacturing experiments. This article also presents the conclusions and other benefits of such laboratory work, as well as possible recommendations for further improvement or expansion.

Keywords: electronics engineering education, laboratory learning environment, learning technology, TCAD tools

RESUMEN

Este artículo describe el análisis de los procesos utilizados en la fabricación de dispositivos de micro y nanoelectrónica. También presenta un ejercicio de laboratorio ejemplar y novedoso en el que se ilustra y analiza paso a paso un transistor bipolar plano *n* + *pn* epitaxial con aislamiento de unión. Solo se utilizan siete pasos de fotolitografía para obtener esta estructura de transistor bipolar: para la formación de capas enterradas, para el aislamiento del transistor de unión y la formación de regiones colectoras, para la formación de regiones base, para la formación de regiones emisoras y colectoras *n*+, para ventanas de contacto, para la primera metalización de aluminio, y finalmente para pasivación. Las herramientas de software Silvaco TCAD se utilizan para implementar todos estos procesos de fabricación y para simular las características I-V resultantes de todas las estructuras de semiconductores presentadas. Este tipo de trabajo de laboratorio proporciona a los estudiantes conocimientos básicos y una comprensión constante de la fabricación de transistores bipolares. Asimismo, este estudio facilita la comprensión teórica, el análisis y la simulación de varios procesos de fabricación de semiconductores sin la necesidad de experimentos de fabricación tecnológicos costosos y largos. Este artículo también presenta las conclusiones y otros beneficios de dicho trabajo de laboratorio, así como posibles recomendaciones para una su mejora o expansión.

Palabras clave: educación en ingeniería electrónica, entorno de aprendizaje de laboratorio, tecnología de aprendizaje, herramientas TCAD

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Introduction

One of the most characteristic features of today's scientific and technical progress is the extent to which electronic devices are used in many human activities, ranging from personal health to public safety, aerospace and defense. The elemental basis of such electronic devices consists of transistors, diodes, resistors, capacitors, and other elements designed and implemented in advanced micro- and later in nano-electronics. Based on recent scientific research, the economic analysis of market trends, and their contribution to social challenges, the European Union's (EU) Key Enabling Technologies (KET) include micro- and nano-electronics, nanotechnology, photonics, advanced materials, industrial biotechnology, and advanced manufacturing technologies (European Commission, 2012). These technologies are an engine of economic and technological development, as well as a major driver of innovation. In 2015, the global KET market was estimated at more than 1 trillion euros, while export of KET products from the EU accounted for up to 23% of exports worldwide. KETs also have great potential for growth and employment: in the coming years, 10-20% of growth potential can be expected (European Commission, 2013; European Commission, 2015). As a result, the European Commission, like other leading economy countries, has developed a strategy to boost the advancement of these high-impact technologies and create new workplaces, thereby boosting growth in other industries and sectors (European Commission, 2018).

At least 10% of the global GDP depends on products and services created by the micro- and nano-electronics industries (Annegarn, *et al.*, 2012). These industries' innovations and their stimulating role is a major driver of growth in all electronics, information technology, automotive, aerospace, medical, and other economic industries. Therefore, the rapid growth of these sectors is also affecting the creation of new workplaces and the need for new employees, with a deeper knowledge. For example, according to the data of the statistical office of the EU (Eurostat), the number of Information and Communication Technology (ICT) professionals covering electronics, information technology, and telecommunications has increased by as much as 39,1% between 2011 and 2018, which is more than 6 times higher than the increase in overall employment of all sectors (6,5%). Similarly, more than two-thirds (63,1%) of ICT professionals in the EU had a university degree (Eurostat, 2018). The United States Bureau of Labor Statistics also projects the need for computer science and ICT professionals. According to forecasts, the employment opportunities of these specialists will increase by 12% between 2018 and 2028, *i.e.* much faster than the average for all other occupations. It is also forecasted that, during this period, about 0,55 million workplaces of this occupation will be created in the USA (United States Department of Labor, 2019).

Such rapid growth and development pose increasingly difficult challenges for higher education institutions. One of the major trials in a rapidly growing industry is to engage and motivate students to study engineering sciences. Most higher education institutions try to solve this problem by giving lectures and various seminars/workshops in secondary schools; organizing events, competitions, and tours with commercial enterprises; improving teacher competencies; and developing effective teaching methods and increasing their diversity. The second challenge, which we mentioned in our previous article and book (Barzdenas, Grazulevicius, and Vasjanov, 2020; Barzdenas, Navickas, 2012) is to provide quality education with minimal or no investment, as the costs of rapidly evolving technologies are very high. These costs, which include capital equipment, human resources, and time, are so expensive that higher education institutions cannot even make a dent with their limited financial resources. For these reasons, teachers are forced to look for virtual software tools that allow at least for the partial replacement of costly equipment. One such tool for virtual simulation of various micro- and nano-electronic structures and devices are various Technology Computer-Aided Design (TCAD) software tools. However, with the help of TCAD software tools, it is necessary to adopt various teaching methods to provide students with interesting tasks to motivate their better understanding of the common and newly developed structures of micro- and nano-electronic devices, as well as their working principles. Therefore, via laboratory projects and lectures, it is advisable to examine examples covering all stages of the manufacturing of these devices, that is, from an unprocessed silicon wafer to the simulation and analysis of the final structure of a semiconductor device and its electrical parameters and characteristics.

In this article, we describe the analysis of the processes used in micro- and nano-electronic device manufacturing. We also an example of a laboratory work where students use Silvaco TCAD software tools to apply a step-by-step approach to the design and simulation of an epitaxial planar $n + pn$ transistor with junction isolation.

Design flow

Bipolar integrated circuits typically use $n + pn$ transistors because their parameters are better than their pnp transistor counterparts. There are two reasons for this. First, the solubility of phosphorus, the impurity of choice for n-type materials, is higher in silicon than that of boron, which is conversely the dopant-of-choice for p-type materials. This leads to a higher impurity density in the emitter region and a higher emitter current transfer coefficient for $n+pn$ transistors. Another reason is that the majority charge carrier of $n + pn$ transistors are electrons whose mobility in silicon is several times higher than that of holes. This results in a higher current transfer coefficient. Additionally, with higher mobility, the transistors have better frequency characteristics and a higher operating speed. Therefore, in the presented laboratory work, we will simulate the manufacturing processes of $n+pn$ bipolar transistors and show supporting Athena and Atlas software code with the explanation of its function.

The purpose of this laboratory work is to simulate the main manufacturing processes of an epitaxial planar $n + pn$ transistor with junction isolation, as well as to extract the I-V characteristics of the obtained semiconductor structure. The

main design stages of the technological process, described below, are as follows: silicon substrate preparation, formation of a n+ buried layer, silicon epitaxial layer growth, formation of junction isolation and collector region, formation of base region, formation of emitter and collector n+ regions, photolithography for contact windows, first aluminum metallization, passivation, description of transistor electrodes, analysis of transistor structure parameters, and simulation of I-V characteristics. All of these twelve stages performed in the laboratory work are shown in Figure 1.

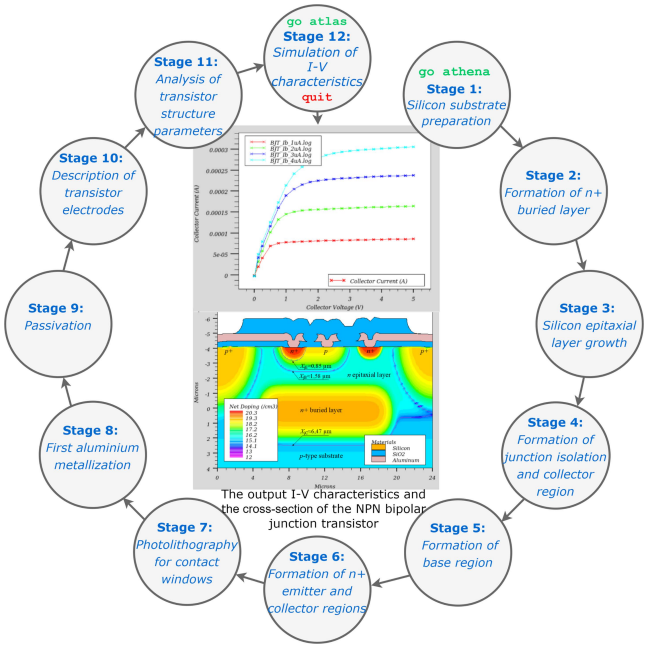

Figure 1. $n + pn$ bipolar junction transistor (BJT) step-by-step manufacturing and analysis flowchart.
Source: Authors

Note: The authors would like to point out that the code below was generated and validated using Silvaco TCAD 2012 software for both Windows and Linux operating systems. It should also be noted that the word lifting symbol (-) in the code in this article means that these lines of code must be interpreted as a single line.

1. *Silicon substrate preparation:* The simulation of a planar epitaxy $n + pn$ bipolar transistor and technological processes of other semiconductor structures with the Silvaco TCAD software can be performed by using the Athena software. This can be done by entering the following program code in the top of the Deckbuild program window:

```
1 # The first line, go Athena, invokes the Silvaco Athena
1 process simulator
2 go athena
```

Simulation of semiconductor structures and their technological processes begins with a description of the silicon wafer's dimensions. Since modern silicon wafers have a maximum diameter of 300 mm or 450 mm, and one transistor has the geometry of several or tens of micrometers, only the part of the wafer where the transistor structures will be formed is selected for simulation. The dimensions of the wafer are indicated along the axes of abscissas and ordinates. Our simulated transistor will have a starting point of the abscissa axis of 0 µm, an end point of 24 µm, and a start point of the ordinate axis of 0 µm and an end point of 4 µm. Later, the mesh (grid line) of the described wafer is formed. This is necessary because Athena uses the finite element method in its calculations. In this method, differential and integral equations are calculated at the intersection of the grid of abscissas and ordinates, so the denser the grid, the more accurate the calculations will be. However, it should be noted that grid density determines the calculation time, *i.e.* the denser it is, the longer the calculation time. Considering the accuracy of the simulation of the transistor structure and the calculation time, the following grid is chosen for further calculations: the abscissa axis will have a step grid of 0,5 µm at 0 µm and 24 µm point, and a denser step grid of 0,1 µm at 6 µm and 18 µm point, since pn junctions of the transistor will be created in this interval. Similarly, in the ordinate axis, a 0,1 µm grid is selected at the wafer's surface, and a 0,5 µm grid at the 4 µm point. The program code for the selected wafer and its grid description is as follows:

```
3 # x dimension definition
4 line x loc=0.0 spacing=0.5
5 line x loc=6.0 spacing =0.1
6 line x loc=18.0 spacing =0.1
7 line x loc=24.0 spacing =0.5
8 # y dimension definition
9 line y loc=0.0 spacing =0.1
10 line y loc=4.0 spacing =0.5
```

Subsequently, the wafer material and its crystallographic structure, doping impurities and their concentration, or the specific resistance ρ of the wafer are indicated. A silicon (Si) wafer with a (100) crystallographic structure, doped with boron and a specific resistance of $\rho = 10\Omega\times$ cm, was chosen. The description code for such a silicon wafer is as follows:

```
11 # (100) silicon wafer doped with boron and having a
11 resistivity of 10 Ω·cm
12 init silicon orient=100 boron resistivity=10 two.d
```

2. *Formation of n+ buried layer:* After preparing the surface of the Si wafer, a 10-minute thermal oxidation process is carried out in an atmosphere of wet oxygen at 1100 °C. The program code for thermal oxidation in wet oxygen is as follows:

```
13 # Wet oxidation at 1100 °C for 10 minutes
14 diffuse time=10 temperature=1100 wetO2 press=2 hcl=3
```

We obtain 0,38 µm thick oxide, which is then coated with a photoresist in a centrifuge. Here, due to centrifugal forces, the photoresist spreads on a flat surface with a thin layer of 0,5 mm uniform thickness. The photoresist coating of the wafer with SiO_2 layer is as follows:

```
15 # The surface is covered with the photoresist AZ1250J
16 deposit name.resist=AZ1350J thickness=0.5 div=10
```

Thereafter, the technological process of photolithography should include the following processing operations: drying,

exposing, heating, developing, and hardening of the photoresist. The photolithography process is replaced by the geometric etching used in Athena to simplify the program code. This etching removes the area of the photoresist specified by the coordinate points. The program code for geometric etching of the photoresist is as follows:

```
17 # Window to form the n+ buried layer
18 etch name.resist=AZ1350J start x=6.0 y=-0.8
19 etch cont x=6.0 y=-0.2
20 etch cont x=18.0 y=-0.2
21 etch done x=18.0 y=-0.8
```

SiO_2 is etched with fluoric acid HF using ammonium fluoride NH_4F as an additive to improve the etching quality. The selectivity of such a mordant to the photoresist is very high (more than 100). The program code for isotropic etching is as follows:

```
22 # Etching speed configurations
23 rate.etch machine=HF wet.etch name.resist=AZ1350J n.m
23 isotropic=1
24 rate.etch machine=HF wet.etch oxide n.m isotropic=100
25 # Etching time setting
26 etch machine=HF time=5 min
```

The remaining photoresist layer is removed in concentrated sulphuric or nitric acid. The removal of the photoresist is described below:

```
27 # Photoresist removal
28 etch name.resist=AZ1350J all
```

It is now possible to perform the initial formation of the n+ buried layer. At a depth of about 0,25 mm of the silicon wafer, a diffusion of arsenic (As) impurities at 1000 °C for 5 minutes is performed:

```
29 # Diffusion of arsenic into the silicon wafer
30 diffusion time=5 temp=1000 c.arsenic=1.0e21
```

After this diffusion, the remaining SiO_2 layer is etched using the following program code:

```
31 # Etching the remaining SiO2 layer
32 etch oxide all
```

3. *Silicon epitaxial layer growth:* An epitaxial layer of 5 μm thick doped with n-type arsenic (N_D = 5 x 10^{15} cm^{-3}) is caused to grow on the wafer by using the chloride method in an epitaxial vertical reactor for 10 minutes at 1000 °C. The program code for this epitaxial process is as follows:

```
33 # Growth of the arsenic-doped silicon epitaxial layer
34  epitaxy time=10 temp=1000 t.final=1100 c.arsenic=5e15
34  thickness=5 div=50
```

4. *Formation of junction isolation and collector region*: The wafer is thermally oxidized, and, during the second photolithography step, windows are etched in the areas where the two-stage boron diffusion will occur. The first diffusion is the doping of boron impurities at 1100 °C for 10 minutes, and the second diffusion is the redistribution of boron impurities at 1200 °C under a dry oxygen atmosphere. The duration of the second stage is chosen so that the boron impurities penetrate the entire thickness of the epitaxial layer. In this way, an n conductivity collector area is isolated by the p+ conductivity areas. The program code for this stage is as follows:

```
35 # Wet oxidation at 1100 °C for 10 minutes
36 diffuse time=10 temperature=1100 wetO2 press=2 hcl=3
37 # The surface is covered with the photoresist AZ1250J
38 deposit name.resist=AZ1350J thickness=0.5 div=10
39 # Window in the photoresist to form the isolation area:
39 left window
40 etch name.resist=AZ1350J start x=0.0 y=-5.6
41 etch cont x=0.0 y=-5.0
42 etch cont x=0.5 y=-5.0
43 etch done x=0.5 y=-5.6
44 # Window in the photoresist to form the isolation area:
44 right window
45 etch name.resist=AZ1350J start x=23.5 y=-5.6
46 etch cont x=23.5 y=-5.0
47 etch cont x=24.0 y=-5.0
48 etch done x=24.0 y=-5.6
49 # Etching speed configurations
50 rate.etch machine=HF wet.etch name.resist=AZ1350J n.m
50 isotropic=1
51 rate.etch machine=HF wet.etch oxide n.m isotropic=100
52 # Etching time setting
53 etch machine=HF time=5 min
54 # Photoresist removal
55 etch name.resist=AZ1350J all
56 # Diffusion of boron into silicon wafer
57 diffusion time=10 temp=1100 c.boron=1.0e21
58 # Redistribution of boron impurities
59 diffusion time=40 temp=1200 dryo2 press=1 hcl=2
60 # Etching the remaining SiO2 layer
61 etch oxide all
```

5. *Formation of base region:* Thermal oxide is grown with a thickness of about 0,38 mm. The third photolithography step is used to open the window of the base of the transistor in the oxide. Through this window, boron diffusion is also carried out in two stages. The target reference parameters of the base layer are: a depth X_{jB} ofabout 1,5-2,0 mm, a sheet resistance R_{sB} of about 250-300 Ω/□, and a surface concentration N_{0B} of about 4-5 x 10^{18} cm^{-3}. During the second stage of diffusion, the oxide layer that has grown in the base area is etched. The program code for this stage is as follows:

```
62 # Wet oxidation at 1100°C for 10 minutes
63 diffuse time=10 temperature=1100 wetO2 press=2 hcl=3
64 # The surface is covered with the photoresist AZ1250J
65 deposit name.resist=AZ1350J thickness=0.5 div=10
66 # Window in the photoresist for base doping
67 etch name.resist=AZ1350J start x=12.5 y=-5.4
68 etch cont x=12.5 y=-4.8
69 etch cont x=17.0 y=-4.8
70 etch done x=17.0 y=-5.4
71 # Etching speed configurations
72 rate.etch machine=HF wet.etch name.resist=AZ1350J n.m
72 isotropic=1
73 rate.etch machine=HF wet.etch oxide n.m isotropic=100
74 # Etching time setting
75 etch machine=HF time=5 min
76 # Removal of the photoresist
77 etch name.resist=AZ1350J all
78 # Diffusion of boron into silicon wafer
79 diffusion time=10 temp=1100 c.boron=3e19
80 # Redistribution of boron impurities
81 diffusion time=15 temp=1200 dryo2 press=1 hcl=2
82 # Etching of the remaining SiO2 layer
83 etch oxide all
```

6. *Formation of emitter and collector n+ regions:* During the fourth photolithography step, windows for emitter diffusion and collector resistance reduction are formed. The n+ emitter is obtained through one-stage diffusion of phosphorus in an oxidizing medium for 5 minutes at 1000 °C. The target reference parameters of the emitter layerare as follows: the depth X_{jE} is about 0,7-0,9 mm, the sheet resistance R_{sE} is about 8–10 Ω/□, and the surface concentration N_{0E} is about 1,5-2,0 x 10^{20} cm^{-3}. The program code for this stage is described below:

```
84 # Wet oxidation at 1100 °C for 10 minutes
85 diffuse time=10 temperature=1100 wetO2 press=2 hcl=3
86 # The surface is covered with the photoresist AZ1250J
87 deposit name.resist=AZ1350J thickness=0.5 div=10
88 # Window in the photoresist for emitter doping
89 etch name.resist=AZ1350J start x=16.0 y=-5.2
90 etch cont x=16.0 y=-4.6
91 etch cont x=17.0 y=-4.6
92 etch done x=17.0 y=-5.2
93 # Window in the photoresist to form the ohmic collector
93 contact
94 etch name.resist=AZ1350J start x=8.0 y=-5.2
95 etch cont x=8.0 y=-4.6
96 etch cont x=9.0 y=-4.6
97 etch done x=9.0 y=-5.2
98 # Etching speed configurations
99 rate.etch machine=HF wet.etch name.resist=AZ1350J n.m
99 isotropic=1
100 rate.etch machine=HF wet.etch oxide n.m isotropic=100
101 # Etching time setting
102 etch machine=HF time=5 min
103 # Photoresist removal
104 etch name.resist=AZ1350J all
105 # Diffusion of phosphorus into silicon wafer
106 diffusion time=5 temp=1000 c.phos=1e21
107 # Etching of the remaining SiO2 layer
108 etch oxide all
```

7. *Photolithography for contact windows:* The silicon wafer is thermally oxidized. The thickness of the oxide is about 0,38 mm. During the fifth photolithography step, windows are etched in areas where the transistor terminals, including the emitter, the base, the collector, and the junction isolation, create ohmic contacts between aluminum and silicon. After the oxide etching, the photoresist is removed. The program code for this stage is as follows:

```
109 # Wet oxidation at 1100 °C for 10 minutes
110 diffuse time=10 temperature=1100 wetO2 press=2 hcl=3
111 # The surface is covered with the photoresist AZ1250J
112 deposit name.resist=AZ1350J thickness=0.5 div=10
113 # Window in the photoresist to form the emitter
113 electrode
114 etch name.resist=AZ1350J start x=16.25 y=-5.1
115 etch cont x=16.25 y=-4.4
116 etch cont x=16.75 y=-4.4
117 etch done x=16.75 y=-5.1
118 # Window in the photoresist to form the base electrode
119 etch name.resist=AZ1350J start x=12.75 y=-5.1
120 etch cont x=12.75 y=-4.4
121 etch cont x=13.25 y=-4.4
122 etch done x=13.25 y=-5.1
123 # Window in the photoresist to form the collector
123 electrode
124 etch name.resist=AZ1350J start x=8.25 y=-5.1
125 etch cont x=8.25 y=-4.4
126 etch cont x=8.75 y=-4.4
127 etch done x=8.75 y=-5.1
128 # Etching speed configurations
129 rate.etch machine=HF wet.etch name.resist=AZ1350J n.m
129 isotropic=1
130 rate.etch machine=HF wet.etch oxide n.m isotropic=100
131 # Etching time setting
132 etch machine=HF time=5 min
133 # Photoresist removal
134 etch name.resist=AZ1350J all
```

8. *First aluminum metallization*: Before covering the aluminum layer through chemical vapor deposition, the wafer is cleaned by means of a chemical or plasma treatment. The projected Al layer thickness is 0,5 mm:

```
135 # Chemical vapor deposition of aluminum
136 rate.depo machine=cvd aluminum n.m cvd dep.rate=250
136 step.cov=0.80
137 deposit machine=cvd time=2 minutes div=10
```

During the sixth photolithography step, windows for the transistor electrodes and other integrated circuit elements such as junction isolation are formed in the photoresist. The aluminum layer is then etched. Conductive paths, which are conductors connecting elements of integrated circuits, remain in the contact windows and on the insulating layer of silicon dioxide. The width of these conductive paths depends on the minimum size of photolithography and/or the maximum densities of the flowing current. Aluminum is etched in acid and alkaline solutions. In the case of a positive photoresist, Al is etched at 60-70 °C in phosphoric acid, and acetic, nitric acid additives are used to improve the etching quality. The etching speed of Al is about 550-600 nm/min, when the mordant solution contains 80% H_3PO_4, 5% HNO_3, 5% CH_3COOH, and 10% deionized H_2O, and the temperature is 60 °C. Then, after removing the photoresist, annealing of the Al contacts is performed at 500 °C to improve the quality of the ohmic contacts. The program code for this stage is as follows:

```
138 # The surface is covered with the photoresist AZ1250J
139 deposit name.resist=AZ1350J thickness=0.5 div=10
140 # Window in the photoresist to form the electrode
141 etch name.resist=AZ1350J start x=10.0 y =-5.6
142 etch cont x=10.0 y=-4.9
143 etch cont x=11.5 y=-4.9
144 etch done x=11.5 y=-5.6
145 # Window in the photoresist to form the electrode
146 etch name.resist=AZ1350J start x=14.5 y =-5.6
147 etch cont x=14.5 y=-4.9
148 etch cont x=15.0 y=-4.9
149 etch done x=15.0 y=-5.6
150 # Etching speed configurations: phosphoric acid
150 solution
151 rate.etch machine=H3PO4 wet.etch name.resist=AZ1350J
151 n.m isotropic=15
152 rate.etch machine=H3PO4 wet.etch aluminum n.m
152 isotropic=550
153 # Etching time setting
154 etch machine=H3PO4 time=1 min
155 # Photoresist removal
156 etch name.resist=AZ1350J all
157 # Surface tension and viscosity of aluminum
158 material aluminum gamma.reflo=860 reflow visc.0=2e-17
158 visc.E=4.45
159 # Aluminum annealing
160 bake time=5 min temp=500 reflow
```

9. *Passivation*: Finally, a continuous layer of silicon dioxide is deposited on the wafer's surface. Subsequently, the passivation photolithography step is performed to open windows for the final contacts/electrodes. These processes conclude the batch processing of transistors and integrated circuits with a

single metallization on a silicon wafer. The program code is as follows:

```
161 # Chemical vapor deposition of SiO2
162 rate.depo machine=SiO2 oxide n.m cvd
162 dep.rate=125 step.cov=0.80
163 deposit mach=SiO2 time=8.0 minute div=10
164 # Photolithography to open the contacts
165 # The surface is covered with the photoresist AZ1250J
166 deposit name.resist=AZ1350J thickness=0.5 div=10
167 # Window in the photoresist to form the emitter contact
168 etch name.resist=AZ1350J start x=0 y=-6.5
169 etch cont x=0 y=-5.9
170 etch cont x=2.0 y=-5.9
171 etch done x=2.0 y=-6.5
172 # Window in the photoresist to form the collector
172 contact
173 etch name.resist=AZ1350J start x=22 y=-6.5
174 etch cont x=22 y=-5.9
175 etch cont x=24.0 y=-5.9
176 etch done x=24.0 y=-6.5
177 # Etching speed configurations
178 rate.etch machine=HF wet.etch name.resist=AZ1350J n.m
178 isotropic=1
179 rate.etch machine=HF wet.etch oxide n.m isotropic=100
180 # Etching time setting
181 etch machine=HF time=10 min
182 # Photoresist removal
183 etch name.resist=AZ1350J all
```

10. Description of transistor electrodes: Once the transistor electrodes are formed, their names need to be specified to simulate the electrical characteristics of the created device. This is done by specifying the midpoints of the following electrodes in the abscissa axis:

```
184 # Electrode names
185 electrode name=collector x=8.5
186 electrode name=emitter x=16.5
187 electrode name=base x=13.0
```

11. Analysis of transistor structure parameters: During the manufacturing of the integrated device, the technological process must be monitored. The quality of oxidation, photolithography, and surface cleaning are visually checked. The parameters of the diffusion area are controlled by measuring sheet resistances R_s, impurity concentrations N_0, and/or junction depths X_j. These parameters can also be fixed with Athena. The depths X_j of the resulting pn junctions at the middle of the emitter, *i.e.* the 16,5 abscissa point (x.val = 16,5) is found using the following program codes:

```
188 # Extraction of the emitter depth XjE
189 extract name="Emitter depth" xj material="Silicon"
189 mat.occno=1 x.val=16.5 junc.occno=1
190 # Extraction of the base depth XjB
191 extract name="Base depth" xj material="Silicon"
191 mat.occno=1 x.val=16.5 junc.occno=2
192 # Extraction of the collector depth XjC
193 extract name="Collector depth" xj material="Silicon"
193 mat.occno=1 x.val=16.5 junc.occno=3
```

The *junc.occno* parameter specifies the order of the semiconductor layers from the substrate surface at the selected point (x.val = 16,5). Since, within the structure of the $n+pn$ transistor, the emitter area is the first layer of the wafer's surface, then *junc.occno* = 1. Meanwhile, the base area is the second layer, and the collector is the third one, so these parameters are set to *junc.occno* = 2, *junc.occno* = 3, respectively.

After the calculations, the following results will be displayed in the bottom executable window of the Deckbuild:

```
EXTRACT > extract name="Emitter depth" xj material="Silicon"
mat.occno=1 x.val=16.5 junc.occno=1
Emitter depth = 0.83842 um from top of first Silicon layer
X.val=16.5
EXTRACT > extract name="Base depth" xj material="Silicon"
mat.occno=1 x.val=16.5 junc.occno=2
Base depth = 1.5771 um from top of first Silicon layer
X.val=16.5
EXTRACT > extract name="Collector depth" xj material="Silicon"
mat.occno=1 x.val=16.5 junc.occno=3
Collector depth = 6.47272 um from top of first Silicon layer
X.val=16.5
```

Calculations show that the emitter's depth (X_{jE}) is approximately equal to 0,84 µm, the base $X_{jB} \approx 1{,}58$ µm, and the collector $X_{jC} \approx 6{,}47$ µm.

The sheet resistances R_s are determined using the following program codes:

```
194 # Extraction of the emitter sheet resistance depth RsE
195 extract name="Emitter sheet resistance" sheet.res
195 material="Silicon" mat.occno=1 x.val=16.5
195 region.occno=1
196 # Extraction of the base sheet resistance depth RsB
197 extract name="Base sheet resistance" sheet.res
197 material="Silicon" mat.occno=1 x.val=13.0
197 region.occno=1
198 # Extraction of the collector sheet resistance depth
198 RsC
199 extract name="Collector sheet resistance" sheet.res
199 material="Silicon" mat.occno=1 x.val=8.5
199 region.occno=1
```

The calculations of the sheet resistance R_s give the following results: $R_{sE} \approx 8{,}92\ \Omega/\square$, $R_{sB} \approx 302{,}93\ \Omega/\square$, $R_{sC} \approx 6{,}84\ \Omega/\square$.

The surface impurity concentrations N_0 of the formed $n+pn$ transistor areas are determined using the following program codes:

```
200 # Extraction of the emitter surface impurity
200 concentration N0E
201 extract name="Emitter surface concentration" surf.conc
201 impurity="Net Doping" material="Silicon" mat.occno=1
201 x.val=16.5
202 # Extraction of the base surface impurity
202 concentration N0B
203 extract name="Base surface concentration" surf.conc
203 impurity="Net Doping" material="Silicon" mat.occno=1
203 x.val=13.0
204 # Extraction of the collector surface impurity
204 concentration N0C
205 extract name="Collector surface concentration"
205 surf.conc impurity="Net Doping" material="Silicon"
205 mat.occno=1 x.val=8.5
```

The calculations of the transistor areas N_0 gives the following results: $N_{0E} \approx 1{,}96 \times 10^{20}$ cm^{-3}, $N_{0B} \approx 2{,}43 \times 10^{18}$ cm^{-3}, collector $N_{0C} = 1{,}82 \times 10^{20}$ cm^{-3}.

Finally, after fixing all the necessary parameters, the designed structure of the n+pn transistor with junction isolation is saved in the file *complete_BJT.str* and represented by the TonyPlot:

```
206 # Saving and plotting of the final structure
207 structure outfile = complete_BJT.str
208 tonyplot complete_BJT.str -set settings.set
```

It should be noted that the TonyPlot has a specified text setting file (*settings.set*). This file stores the graph settings, text sizes, label names, etc. Therefore, when a Tonyplot graph is configured for the first time, this information is saved and reused as a template when creating new graphs and images. An example of this file is provided in Appendix A at the end of this article.

When all commands discussed above are saved in the Deckbuild program window, calculations are performed. During this process, the TonyPlot will show the structure of a planar epitaxial bipolar $n+pn$ transistor and the impurity distribution in the semiconductor volume. It can be seen in Figure 2.

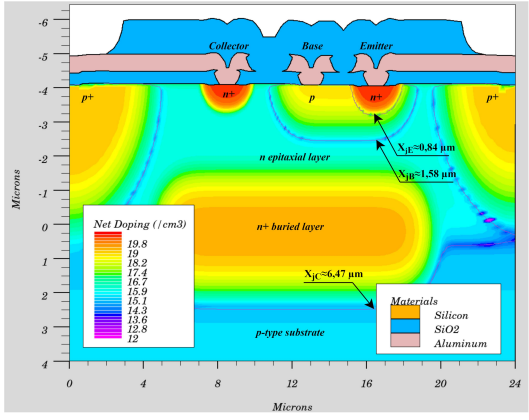

Figure 2. Cross-section view of the $n + pn$ bipolar junction transistor.
Source: Authors

Previously, X_j setup program codes were provided, but this can also be done graphically. To do this, select the sequence of commands *Plot* → *Display* → *Junction* in the TonyPlot window, and when it is executed, *pn* junction boundaries will be plotted. To set these boundaries accurately, it is advisable to use a ruler that can be selected by executing the *Tools* → *Ruler* command sequence. After making measurements at the middle of the emitter, *i.e.* at 16,5 µm abscissa point, it can be seen that $X_{jE} \approx 0{,}84$ µm, $X_{jB} \approx 1{,}58$ µm, and $X_{jC} \approx 6{,}47$ µm. The results of the measurements are presented in Figures 2 and 3.

The *Tools* → *Cutline* command sequence is used to determine the impurity distribution in the desired areas of the semiconductor structure. After executing this command and selecting the vertical cursor, the desired point of the abscissa axis (in this case, the middle of the emitter, x = 16,5 µm) generates a graph of the net doping Neff (Figure 3). Neff is the modulus of the difference between donor N_D and acceptor N_A impurities, *i.e.* $N_{eff} = |N_D\text{-}N_A|$. This graph can also be used to determine the X_j depths of *pn* junctions. Knowing that *pn* junctions are formed at a depth where the concentration of doped donor impurities is equal to the concentration of acceptor impurity (*i.e.* $N_{eff} = |N_D\text{-}N_A| = 0$), the minima of this graph will correspond to the previously calculated and measured values of X_{jE}, X_{jB}, and X_{jC}.

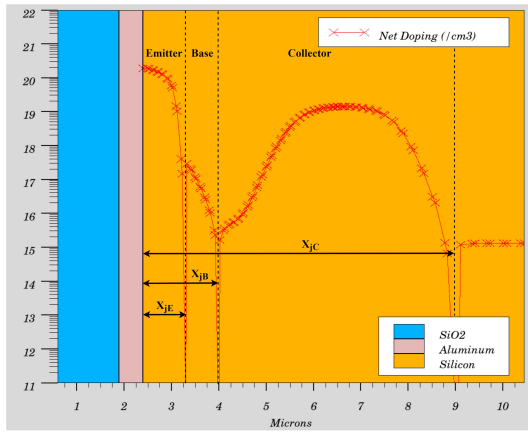

Figure 3. Doping profiles of the $n + pn$ bipolar junction transistor.
Source: Authors

12. *Simulation of I-V characteristics:* Here is the program code for simulation of the output I-V characteristics family of a planar epitaxial bipolar $n + pn$ transistor:

```
209 # The first line, go Atlas, invokes the Silvaco Atlas
209 device simulator
210 go atlas
211 # Loading of the n+pn bipolar transistor structure
212 init infile=complete_BJT.str
213 # Description of bipolar transistor models
214 models conmob fldmob consrh auger print
215 # Setting of the base current values
216 solve init
217 solve vbase=0.1 vstep=0.1 vfinal=0.7 name=base
218 contact name=base current
219 solve ibase=1.e-6 outfile=BJT_1uA
220 solve ibase=2.e-6 outfile=BJT_2uA
221 solve ibase=3.e-6 outfile=BJT_3uA
222 solve ibase=4.e-6 outfile=BJT_4uA
223 # Changing the collector voltage at a given base
223 current
224 load infile=BJT_1uA
225 log outfile=BJT_1uA.log
226 solve vcollector=0.0 vstep=0.25 vfinal=5.0
226 name=collector
227 load infile=BJT_2uA
228 log outfile=BJT_2uA.log
229 solve vcollector=0.0 vstep=0.25 vfinal=5.0
229 name=collector
230 load infile=BJT_3uA
231 log outfile=BJT_3uA.log
232 solve vcollector=0.0 vstep=0.25 vfinal=5.0
232 name=collector
233 load infile=BJT_4uA
234 log outfile=BJT_4uA.log
235 solve vcollector=0.0 vstep=0.25 vfinal=5.0
235 name=collector
236 # Saving and plotting of the output I-V
236 characteristic-curve
237 tonyplot -overlay BJT_1uA.log BJT_2uA.log BJT_3uA.log
237 BJT_4uA.log -set BJT_settings.set
238 quit
```

An example of the *BJT_settings.set* settings file is given in Appendix B.

Figure 4 shows the family of the output I-V characteristics of a bipolar $n + pn$ transistor. These characteristics show that the current of the collector I_C is controlled by the current of the base I_B. When V_C = 2 V, and when the I_B current changes from 1 µA to 2 µA, the collector current I_C increases from 50

μA to 100 μA, that is, the base current transfer coefficient β is about 50.

Conclusions

The design and analysis of the manufacturing processes were performed for an epitaxial planar $n + pn$ bipolar transistor with junction isolation, using only the seven photolithography steps. The basic design parameters of the transistor are given below. The crystallographic orientation of the silicon wafer is (100), doped with boron, and the specific resistance is ρ = 10 Ω x cm. The epitaxial layer of silicon is 5 μm thick, n-type, and has a surface concentration of $N_D = 5 \times 10^{15}$ cm^{-3}. The depth of the emitter is approximately equal to $X_{jE} \approx 0{,}84$ μm, the base $X_{jB} \approx 1{,}58$ μm, and the buried layer (collector) $X_{jC} \approx 6{,}47$ μm. Sheet resistance is, respectively, $R_{sE} = 8{,}92$ Ω/□, $R_{sB} = 302{,}93$ Ω/□ and $R_{sC} = 6{,}84$ Ω/□, and the surface concentrations $N_{0E} \approx 1{,}96 \times 10^{20}$ cm^{-3}, $N_{0B} \approx 2{,}43 \times 10^{18}$ cm^{-3}, and $N_{0C} = 1{,}82 \times 10^{20}$ cm^{-3}, respectively.

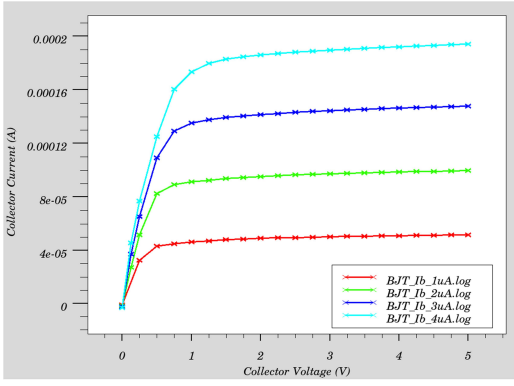

Figure 4. Output I-V characteristics of the n+pn bipolar junction transistor.
Source: Authors

Discussions

At first glance, this kind of laboratory work may be considered 'dry', when merely entering the specified program code and realizing the supplied transistor structure without much further consideration. If students mechanically or monotonously enter the program code without delving into its meaning, syntax, and sequence, they do not acquire new knowledge, and, thus, the laboratory work becomes boring for them. To avoid this scenario, it is also necessary to present additional interesting tasks or control questions or tests that will allow students to understand the essence of this laboratory work and consolidate their knowledge. Therefore, each laboratory work session should be divided into separate stages that define the basic steps or groups of steps in the manufacturing of the micro- and nano-electronics device being developed. For example, the laboratory work presented in this article distinguishes 12 main stages: silicon substrate preparation, formation of a n+ buried layer, silicon epitaxial layer growth, formation of junction isolation and collector region, formation of base region, formation of emitter and collector n+ regions, photolithography for contact windows, first aluminum metallization, passivation, description of transistor electrodes, analysis of transistor structure parameters, and simulation of I-V characteristics. All these stages are shown in Figure 1. At each of these stages, the student is given additional tasks, which are presented in the form of a test. These tasks include both theoretical questions that examine the student's knowledge gained during the lectures and practical questions/tasks, which allows them to assess their skills and understanding. For example, in the silicon substrate preparation stage, students are asked test questions about the silicon monocrystalline ingot growth technologies, the slicing methods of the silicon ingot, the standard wafer diameters and thickness, the basic process steps for wafer preparation, and similar questions, which are discussed in detail during the lectures. Meanwhile, the practical questions ask a variety of questions related to the TCAD program code that were performed during laboratory work: how the dimensions of the silicon wafer are described, what the purpose of the mesh and its density is, among others. Practical questions also include asking students to create teacher-provided examples of silicon wafers with an appropriate or specific mesh. Meanwhile, in the final simulation of I-V characteristics, students answer theoretical questions related to the physical phenomena of BJTs, their regions of operation, different configurations for connecting BJTs, transistor testing methods, and so on. This article presents the program code for the output I-V characteristics family of BJTs. However, with a simple modification of this program code, the input I-V characteristics family can be obtained. Such modifications are given to students in practical tasks. From the obtained I-V characteristics, students can determine the basic parameters of BJTs: the common-emitter current transfer factor β, saturation and cut-off voltage points, transconductance, early voltage point, and others. The ability to simulate and analyze the I-V characteristics of transistors enables students to understand the theory of transistor operation, their basic parameters, and the technical specifications provided by manufacturers. This acquired knowledge and abilities allow students to properly use bipolar transistors to design various electronic devices.

After completing all these additional tasks, the student gets an assessment and proceeds to the next stage of this laboratory work. By completing all the stages and additional tasks, the student gets a final total grade.

Since these tasks do not require complex and expensive equipment, but only software tools, they can also be done remotely. In the case of most TCAD software packages, students can log in to their dedicated accounts or use licenses for these software tools remotely. Distance learning opens a wide range of opportunities for students and teachers alike. Students can learn and complete tasks with their own potential and at their own pace and time, and teachers, in turn, can come up with more interesting homework, course projects, or complex tasks that involve teams of students. This will enable students to further expand their knowledge and gain new research and experimentation experience while developing project management and people skills.

As mentioned earlier, teachers can also provide interesting

course projects that students can do individually or in teams. For these projects, it is appropriate to give tasks from scientific publications that provide images or photos of real micro- and nano-electronic device structures. Students make an accurate computer simulation of these structures and analyze the obtained results by using the TCAD software tools and data from scientific publications. Two main advantages of such tasks could be highlighted. The first advantage is that students are convinced of the simulation accuracy of the TCAD software tools, and the second advantage is that students analyze scientific literature, which promotes scientific cognition and allows students to evaluate the possibilities of the practical application of scientific achievements. An example of one simple course project is shown in Figure 5.

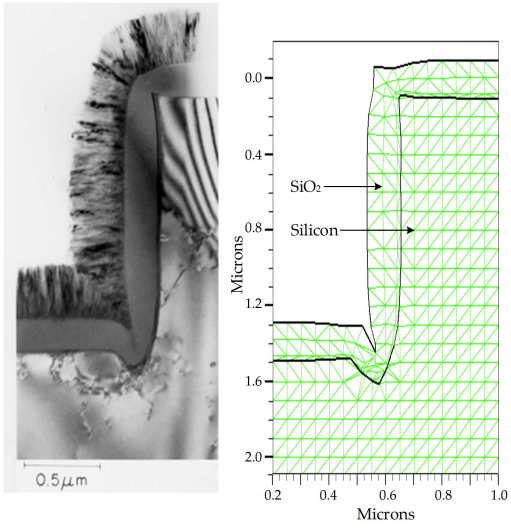

Figure 5. Oxidation in wet oxygen at 950 °C for 40 minutes: a) semiconductor structure photo (Marcus and Sheng, 1982); b) results of TCAD computer simulation.
Source: Authors

This figure shows the growth specificity of silicon oxide, which depends on surface relief, various defects, and the formation of stresses. Students select appropriate materials and technological process parameters specified in the scientific article, and they simulate this structure and perform analysis with TCAD software tools. The results of this effort are submitted to the lecturer and presented to other students.

Valuable references which can be used as sources of theoretical material when coming up with tasks for students can be found in the referenced books and publications (Armstrong and Maiti, 2007; Maiti and Maiti, 2013; Maiti, 2017; Plummer, Deal, and Griffin, 2000; Sarkar, 2013).

This type of laboratory work, along with proposed tasks and control questions or tests, has been positively received by students at the Vilnius Gediminas Technical University. We have disclosed this in our previous article (Barzdenas, Grazulevicius, and Vasjanov, 2020) by providing capturing student feedback over several years. At the end of each laboratory work, a voluntary student survey is conducted to collect immediate feedback. Figure 6 and Table 1 show a subset of eight questions from this questionnaire. The answers of 83 fifth-year respondents were collected. For example, 81,93% and 85,54% of the respondents answered positively to the questions "Did you like carrying out this lab work?" and "Did this lab work provide you with new knowledge or skills?". Such a large number of positive responses indicates that students are both particularly receptive about the use of such laboratory work in the study process, and that it promotes the assimilation of the theoretical material introduced during lectures.

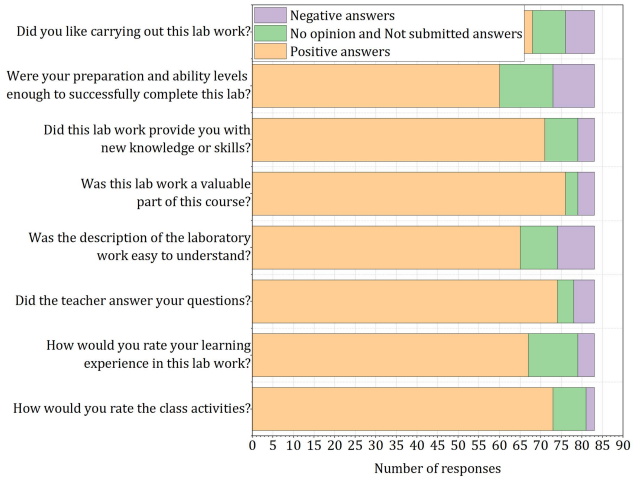

Figure 6. Graphical representation of the survey results.
Source: Authors

Table 1. Summary of the student survey results, $N = 83$

Question	Positive answers	No opinion and not submitted answers	Negative answers
How would you rate the class activities?	73	8	2
How would you rate your learning experience in this lab work?	67	12	4
Did the teacher answer your questions?	74	4	5
Was the description of the laboratory work easy to understand?	65	9	9
Was this lab work a valuable part of this course?	76	3	4
Did this lab work provide you with new knowledge or skills?	71	8	4
Were your preparation and ability levels enough to successfully complete this lab?	60	13	10
Did you like carrying out this lab work?	68	8	7

Source: Authors

Conclusions

This paper presents an exemplary laboratory work cycle of manufacturing processes for micro- and nano-electronics

devices. The aim of this laboratory work is to simulate the structure and I-V characteristics of an epitaxial planar $n + pn$ bipolar transistor with junction isolation using Silvaco TCAD software tools. Seven photolithography steps were used to obtain the structure of this transistor: buried layer formation, junction transistor isolation and collector region formation, base region formation, emitter and collector $n+$ region formation, contact windows, first aluminum metallization, and passivation. This laboratory work also provides examples of the determination of sheet resistances, surface impurity concentrations, and junction depths of individual regions of the resulting bipolar transistor. Such laboratory work, which covers all device manufacturing processes and the simulation of their electrical characteristics, enables students to have a consistent view of the manufacturing process of such devices in order for them to deepen their knowledge gain new research and experimentation experience. In turn, this knowledge and these skills will enable students to contribute significantly in the future to the ever-growing development of micro- and nano-electronics and other industries and sectors.

Appendix A

```
### Semiconductor structure image/view settings ###
# View mesh on/off
show mesh off
# Material edges enabled/disabled
show edges on
# Materials display on/off
show materials on
# Impurity concentration distributions on/off
show contours on
# Junction depths on/off
show junctions on
### Settings of impurity concentrations ###
# Show the effective impurity concentration
contours 1 impurity "Net Doping"
# Show impurity concentrations in silicon only
contours 1 materials 1
contours 1 materials "Silicon" 1
# Color step of impurity concentration divisions
contours 1 nsteps 33
# Impurity concentrations outline on/off
contours 1 outline off
# Color palette of impurity concentrations
contours 1 color 0
# Enable impurity concentration settings
contours 1 apply
```

Appendix B

```
### Label position settings ###
# Collector current label at the bottom right
key electrical at 1
# Base currents label at the top left
key overlay at 4
# Enable label position settings
key apply
### Output I-V characteristics graph settings ###
# Show graph points
show points on
# Show graph lines
show lines on
# Graph type setting
xygraph type 0 convert 0
# Graph y-axis scale setting
xygraph yaxis scale linear
# x-axis type setting
xygraph xaxis "Collector voltage" linear
# y-axis type setting
xygraph yaxis "Collector current" linear
# Show x-axis title
show label xaxis on
# Show y-axis title
show label yaxis on
# x-axis title description
label xaxis "Collector voltage, V"
# y-axis title description
label yaxis "Collector current, A"
```

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Verification of a Fabless Device Model Using TCAD Tools: from Bipolar Transistor Formation to I-V Characteristics Extraction

Verificación de un modelo de dispositivo sin defectos utilizando herramientas TCAD: desde la formación de transistores bipolares hasta la extracción de características I-V

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