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Numerical and Experimental Comparison of the Control Techniques Quasi-Sliding, Sliding and PID, in a DC-DC Buck Converter

Comparación numérica y experimental de técnicas de control quasi-sliding, sliding y PID en un convertidor buck.

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***Resumen*—En este artículo son aplicadas varias técnicas de control para un convertidor reductor DC-DC estas son: control por modos deslizantes (SMC), PID y promediado de dinámica cero (ZAD). El comportamiento en el tiempo para cada controlador es mostrado tanto numéricamente como experimentalmente. Los resultados de SMC y PID son contrastados con la estrategia de control ZAD-FPIC esta última es combinada con una reciente técnica de control llama FPIC (control por inducción al punto fijo). La estabilidad de SMC es garantizada mediante teorema de Lyapunov. El control PID es diseñado de forma analítica usando desplazamiento de polos. El principal problema en la realización experimental fue la velocidad de muestreo y retención de las variables adquiridas del sistema, adicionalmente el tiempo de retardo presente en los procesos de procesamiento. Desde el punto de vista práctico la técnica de control ZAD-FPIC tiene ventajas en comparación con PID y SMC cuando se trabaja con muestreo y retención, esas ventajas han sido corroboradas experimentalmente. Los experimentos han sido probados en sistema RCP (prototipo rápido de control) específicamente en una DSP de la compañía dSPACE, al final tanto los resultados de la simulación numérica y la experimental son muy similares.**

***Palabras clave*—Control por modos delizantes, ZAD-FPIC, diseño de control analítico PID, resultados numéricos y experimentales, retardo de tiempo, DPWM, convertidor DC-DC reductor, análisis de estabilidad por Lyapunov.**

***Abstract*— In this paper the Sliding Mode Control (SMC), PID and ZAD (Zero Average Dynamic) strategies are applied to an electronic DC-DC power converter. Time behavior for each controller is shown for numerical solution and experimental realization. The results in SMC and PID are contrasted with a ZAD-FPIC controller combined with a recently developed strategy named FPIC (Fixed Point Induction Control). Stability in SMC is guaranteed by the Lyapunov theorem. The PID controller is designed in an analytical way using pole placement. The main problem with the physical realization was the sample and hold in the variable acquisition system, in addition to time delay introduced by the computing process. From a practical point of view, the ZAD-FPIC technique has advantages no shown by PID and SMC working with sample and hold, these advantages have been corroborated experimentally. The designs have been tested in an RCP (Rapid Control Prototyping) system based on DSP from the dSPACE platform. Both numerical performance and experimental performance agree.**

***Key Word* —Sliding mode control, ZAD-FPIC, PID controller analytical design, numerical and experimental results, delay time, DPWM, DC-DC buck converter, Lyapunov analysis.**

I. INTRODUCTION

Nowadays, digital PWM (DPWM) is increasingly used for control electronic power converters. This is because it has, because of a number of potential advantages, including: programmability, ability to interface with digital systems, a potentially faster design process, lower sensitivity to parameter variations, reduction or elimination of external passive components, calibration or protection algorithms. Likewise the possibility of implementing nonlinear control techniques in order to improve dynamic responses has been highlighted as a potential advantage of digital control [1], [2], [3]. DPWM has enabled practical realizations of high frequency digital controllers for dc-dc converters (e.g., [4], [5]). In [6] a nonlinear control, which is triggered every T period, is presented.

However, the DPWM also has disadvantages. It is affected by two limitations: quantization effects [7], [8], namely the A/D

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converter, and delays in the control loop [9]. These can cause undesirable limit-cycle oscillations. In [2] the presence of steady-state limit cycles in DPWM converters is discussed, and conditions on the control law and the quantization resolution for their elimination are suggested. In [1] an approach to improve dynamic responses of digitally controlled DC-DC converters using no uniform analog-to-digital (A/D) quantization of the output voltage error is presented.

Due to the high cost of Digital Signal Processor (DSP), applications are limited to high power applications like motor drives and expensive systems. In [3] a diagrammatic method to find out a minimum requirement of digital controller with considerations on both time sampling and quantization resolution dimensions is provided.

Nowadays, the ZAD control technique has been studied in the literature [6, 10, 11, 12]. In particular, in [10] the transition to chaos was found through analytical and numerical results, as the parameter Ks varied, on the other hand, the development and application of a new control technique FPIC (Fixed Point Induction Control) has been shown in [11, 12, 13, 14, 15, 16]. This technique allows us to stabilize unstable orbits in a simple way. In [16] introduce the load estimator by means of LMS, to make ZAD and FPIC control feasible in load variation conditions.

In this paper the Sliding Mode Control (SMC), PID and ZAD (Zero Average Dynamic) strategies are applied at a DC-DC buck converter. The results in SMC and PID are contrasted with a ZAD controller combined with a recently developed strategy named FPIC. The designs have been tested in a DSP from the dSPACE platform. Both numerical performance and experimental performance agree.

The paper is organized as follows: section 2 describes the proposed model. Section 3 describes mathematical considerations of the system and the SMC, PID and ZAD-FPIC strategies. Section 4 is devoted to the results and finally, section 5 presents the conclusions.

II. PROPOSED MODEL

Figure (1) shows the global system, the software part is fully realized in a DSP (DS1104) using Matlab-Simulink and executed in real time. The hardware was implemented with electronic component and buck power converter with parasitic elements is shown in Figure (2). Output voltage regulation $\upsilon_c = V_o$ can be done with this configuration, V_{fd} is the diode forward voltage, r_s, r_M , r_{Med} , r_L, are the internal resistance of the source, the MOSFET, the current sensor and the inductor, respectively.

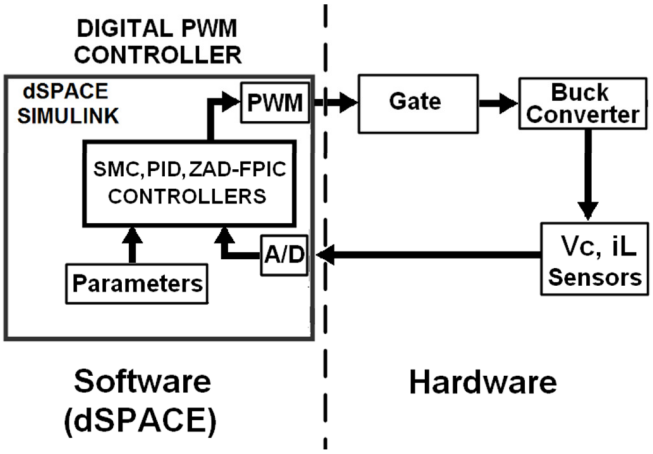

Figure 1. Block diagram of experiment for SMC, PID and ZAD-FPIC controllers.

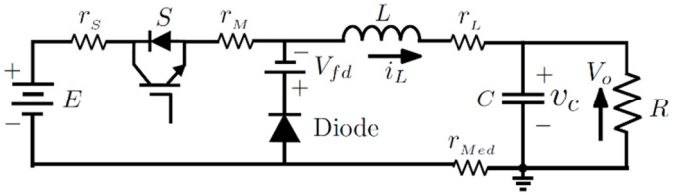

Figure 2. Buck power converter.

III. MATHEMATICAL CONSIDERATIONS

In this section, we present the general tools needed to analyze and control the power converter.

A. SYSTEM MODEL.

This system can be expressed in a mathematical way by the following set of differential equations: when the switch is ON, it is described by equation (1); when the switch is OFF, it is described by equation (2).

$$\dot{\upsilon}_c = \frac{-1}{RC}\upsilon_c + \frac{1}{C}i_L + \frac{0}{C}E$$

$$\dot{i}_L = \frac{-1}{L}\upsilon_c + \frac{-(r_s + r_M + r_{Med} + r_L)}{L}i_L + \frac{1}{L}E \quad (1)$$

$$\dot{\upsilon}_c = \frac{-1}{RC}\upsilon_c + \frac{1}{C}i_L + \frac{0}{C}V_{fd}$$

$$\dot{i}_L = \frac{-1}{L}\upsilon_c + \frac{-(r_{Med} + r_L)}{L}i_L + \frac{-1}{L}V_{fd} \quad (2)$$

The equations (1) and (2) they can be written in this way $\dot{x} = Ax + Bu$ with $x_1 = \upsilon_c$ and $x_2 = i_L$. The control scheme used in this work corresponds to a Centered Pulse Width Modulation (CPWM) [13, 14, 16, 19]. The system operates as:

$$\dot{x}=\begin{cases} A_1x+B_1 & \text{if} \quad kT\le t\le (k+d_k/2)T \\ A_2x+B_2 & \text{if} \quad (k+d_k/2)T<t<(k+1-d_k/2)T \\ A_1x+B_1 & \text{if} \quad (k+1-d_k/2)T\le t\le (k+1)T \end{cases} \quad (3)$$

Where d_k is the duty cycle, and it is obtained as $d_k = D_k / T$, with $T = 200\,\mu s$ is the sampling time and D_k is the duty cycle into range the 0 at 1.

B. SLIDING MODE CONTROL TECHNIQUE

The advantages of this control structure lie in the fast dynamic response and high robustness with respect to disturbances and parameter variations [17].

Let $x_{1ref} = \upsilon_{ref}$ be the reference of output voltage and (4) the voltage tracking error.

$$e = x_{1ref} - x_1 \quad (4)$$

Define state variables $z_1 = e$ and $z_2 = \dot{e}$. The υ_c equation of the DC buck converter (1) with respect to the states z_1, z_2 is given by

$$\dot{z}_1 = z_2$$

$$\dot{z}_2 = -a_1z_1 - a_2z_2 + f(t) - bu(t) \quad (5)$$

Where $a_1 = 1/(LC) + (r_s + r_M + r_{Med} + r_L)/(RLC)$, $a_2 = 1/(RC) + (r_s + r_M + r_{Med} + r_L)/L$, $b = 1/(LC)$ are constant values. The linear part of (5) is perturbed by $f(t) = \ddot{\upsilon}_{ref} + a_2\dot{\upsilon}_{ref} + a_1\upsilon_{ref}$, depending on the desired output voltage υ_c. Since (5) is a second order system, the switching function is designed as:

$$s = cz_1 + \dot{z}_1 \quad (6)$$

With c being a positive constant. The associated controller is defined as:

$$u = u_0 sign(s) \quad (7)$$

Where u_0 is the link voltage. According to these equations, the voltage tracking error z_1 decays exponentially after the sliding mode occurs in the manifold $s = cz_1 + \dot{z}_1 = 0$. Where constant c determines the rate of the convergence. The system motion in sliding mode is independent of parameters a_1, a_2, b and disturbances in $f(t)$.

When the output trajectory is not on the sliding surface $s(t)$ the controller must drive the output trajectory to the sliding mode $s(t) = 0$. The system under this condition is said to be on the reaching phase. For this purpose, the Lyapunov function is selected as:

$$V(t) = \frac{1}{2}s^2(t)$$

The

$$\dot{V}(t) = s(t)\dot{s}(t)$$

To enforce the sliding mode, control gain u_0 should be selected so that $s(t)\dot{s}(t) < 0$.

$$s(t)\dot{s}(t) = s(c\dot{z}_1 + \dot{z}_2) < 0$$
$$s(t)\dot{s}(t) = s(cz_2 - a_1z_1 - a_2z_2 + f(t) - bu(t)) < 0$$
$$s(cz_2 - a_1z_1 - a_2z_2 + f(t)) < bsu(t)$$

For the control command $u = u_0 sign(s)$

$$s(cz_2 - a_1z_1 - a_2z_2 + f(t)) < bu_0 s\, sign(s)$$
$$\left|s(cz_2 - a_1z_1 - a_2z_2 + f(t))\right| < bu_0\left|s\right|$$

Then the link voltaje u_0 should satisfy the condition

$$u_0 > \frac{1}{b}\left|cz_2 - a_1z_1 - a_2z_2 + f(t)\right| \quad (8)$$

For sliding mode to exist. Then, after a finite time interval, the system status will reach the sliding manifold $s(t) = 0$. Thereafter, the system response depends only on the design parameter c.

Figure (3) shows the SMC control simulation diagram on Matlab-Simulink, using (6) and (7). In figure lowest part the A/D converter is simulated with Zero-Order Hold, 12 bits

Quantizer and Unit Delay. In 9 bits Quantizer block the quantization effect over DPWM generator is considered.

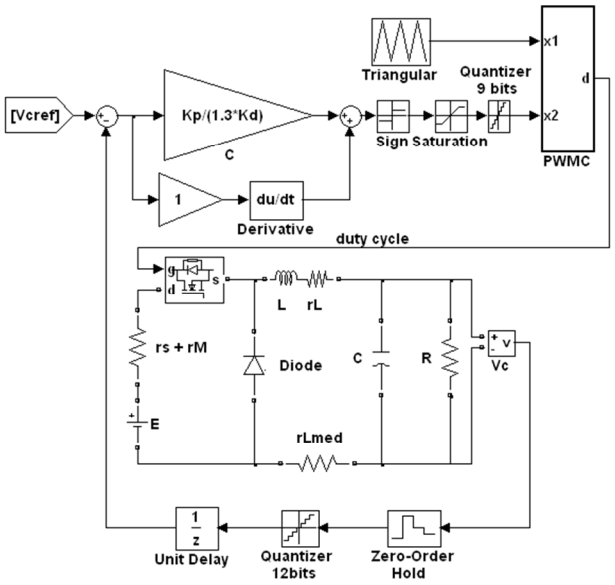

Figure 3. Sliding Mode Control simulation.

C. PID CONTROLLER.

For the PID controller design, a pole placement method is used, It starts with a desired behavior, determined by the second order canonical equation, which should match the characteristic equation of the closed loop system with PID to find the constants Kp, Kd, Ki.

For desired response $ts = 0.6$ ms, $Mp = 1\%$.

$\zeta = 0.8261,\ \omega_n = 8070.2$

Second order canonical equation (desired behavior):

$$\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\frac{8070.2^2}{s^2 + 13333.58s + 8070.2^2}$$

With poles on:

$$-6666.67 \pm j4547.9$$

In the case where the switch is closed, in buck converter model (1), we can rewrite the state equation as:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ b_{21} \end{bmatrix} u \quad (9)$$

$$y = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

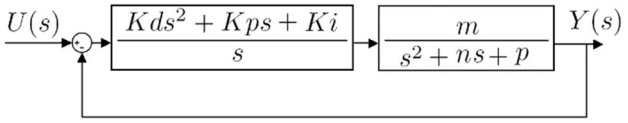

Figure 4
Closed loop system with unknown parameters.

Where $a_{11} = -1/RC$, $a_{12} = 1/C$, $a_{21} = -1/L$, $a_{22} = -(r_s + r_M + r_{Med} + r_L)/L$, $b_{21} = 1/L$, $x_1 = \upsilon_c$, $x_2 = i_L$ and $u = E$.

The transfer function using:

$$G(s) = \frac{Y(s)}{U(s)} = C(SI - A)^{-1}B$$

(10)

Yields:

$$G(s) = \frac{b_{21}a_{12}}{s^2 - (a_{11} + a_{22})s + (a_{11}a_{22} - a_{12}a_{21})} \quad (11)$$

In equation (11), the following values will be replaced to find the system's response:

$$E = 40.086\,V; \quad C = 46.27\,\mu F$$
$$R = 40\,\Omega; \quad r_s + r_M = 0.6887\,\Omega \quad (12)$$
$$L = 2.473\,mH; \quad r_{Med} + r_L = 1.345\,\Omega$$

$$G(s) = \frac{8739294.7}{s^2 + 1362.6684s + 9183623.044} \quad (13)$$

The poles of equation (13) are:

$$-681.3 \pm j2952.9$$

Closed loop with unknown PID constants: when replacing the parameters in the transfer function and making a change of variables $m = 8739294.7$, $n = 1362.6684$, $p = 9183623.044$, you must close the loop with unknown PID as shown in Figure (4). This yields the transfer function with the unknowns constants of PID:

$$Glc(s) = \frac{mKds^2 + mKps + mKi}{s^3 + (n + mKd)s^2 + (p + mKp)s + mKi} \quad (14)$$

In the transfer function (14) there are zeroes that must be canceled so that the system behavior will be equal to the

desired transfer function. For this purpose the gain (15) must be cascaded with $Glc(s)$ (14).

$$Gf(s) = \frac{mKi}{mKds^2 + mKps + mKi} \quad (15)$$

Then

$$G_T(s) = \frac{mKi}{s^3 + (n + mKd)s^2 + (p + mKp)s + mKi} \quad (16)$$

Is obtained.

For matching the characteristic equations, the degree of the desired second order characteristic equation must be increased. This is done by adding a remnant pole so as not to affect the desired behavior significantly.

$$(s + 35000)(s^2 + 13333.58s + 8070.2^2) \quad (17)$$

The coefficients can be calculated by matching the denominator of (16) with (17):

$$(n + mKd) = 4833.4 \Rightarrow Kd = 0.00537473$$
$$(p + mKp) = 5.3179 * 10^8 \Rightarrow Kp = 59.80029 \quad (18)$$
$$(mKi) = 2.2795 * 10^{12} \Rightarrow Ki = 260831.5848$$

Replacing these constants (18) in the closed loop transfer function (16), then the simulation is performed with a step value of E volts. Figure (5) shows the block diagram for PID control simulation.

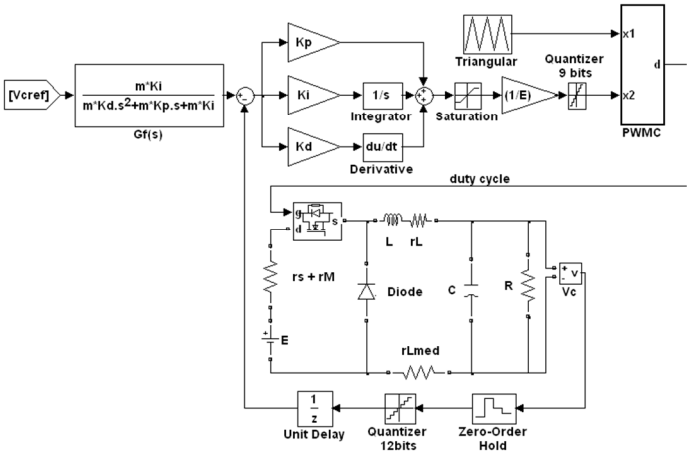

Figure 5. PID control simulation.

D. ZAD-FPIC CONTROL TECHNIQUE.

This control technique was proposed by [6], numerically and experimentally tested in [12, 13, 18, 19]. A complete discussion on the design of the ZAD-FPIC controller is presented in [13, 15, 16].

The duty cycle is calculated as follows [13, 19]:

$$d = \frac{d_k + N.\, d^*}{N + 1} \quad (19)$$

Where d_k is the duty cycle calculated in each iteration and d^* is calculated at the beginning of each period as follows:

$$d^* = T\left[\frac{x_{1ref}(1 + \frac{r_{Med} + r_L}{R}) + V_{fd}}{-x_{1ref}(\frac{r_s + r_M}{R}) + E + V_{fd}}\right] \quad (20)$$

The equation (19) incorporates ZAD and FPIC techniques. Figure (6) shows the block diagram for the ZAD-FPIC control simulation taking into account load estimator presented by [16] p. 4.

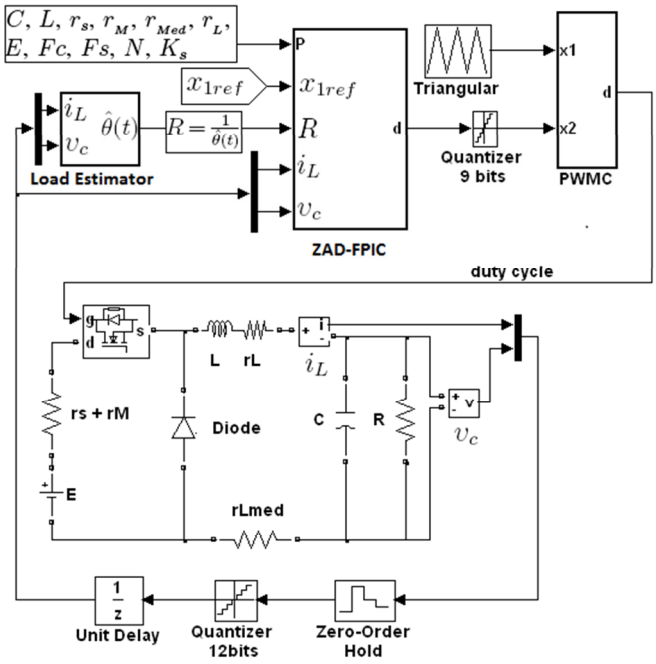

Figure 6. ZAD-FPIC control simulation.

IV. RESULTS OF THE CONTROLLED BUCK CONVERTER WITH THE PROPOSAL TECHNIQUES.

In Table (1) the parameters of buck converter for the three controllers are shown, figures (7), (8), (9) and (10) shows the performance of the control techniques for the continuos case. The parameters for the PID were calculated in equation (18), but the Ki and Kd were changed to $Ki = 0.67Ki = 130415.7924$ and $Kd = 1.2Kd = 0.00644967$ respectively in order to compensate for saturation effects. The SMC parameter c was tuned by $c = Kp/(1.3 * Kd) = 8558.6109$ to get a behavior like that of the PID controller. The ZAD-FPIC

technique was implemented using equation (20) and the parameters of Table (1) with $Ks=1$ and $N=1$. Figure (8) shows the percentage error obtained by control techniques compared. The SMC also has better stability and all controllers have lower steady-state error.

Load variations in the controller is shown in Figures (9), (10). The load was changed from $R=40\Omega$ to $R=10\Omega$ to $t=4\ ms$. Then, in ZAD-FPIC, a load estimator presented by [16] is necessary, the best controllers to load changes is the SMC and ZAD-FPIC.

TABLE I
SYSTEM PARAMETERS

Parameter	Description	Value
R	Load resistance	40 Ω
C	Capacitance	46.27 μF
L	Inductance	2.473 mH
r_s	Internal resistance of the source	0.3887 Ω
r_M	MOSFET conduction resistance	0.3 Ω
r_{Med}	Current measurement resistance	1.007 Ω
r_L	Internal resistance of the inductor	0.338 Ω
E	Input voltage	40.086 V
F_C	Switching frequency	5 kHz
F_s	Sampling frequency	5 kHz

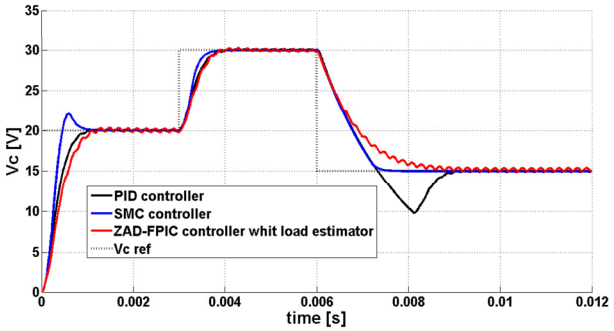

Figure 7. Performance control techniques.

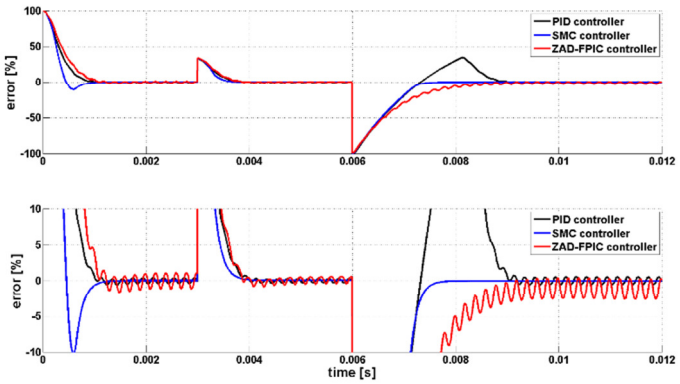

Figure 8. Error obtained by control techniques.

Figure (10) shows the duty cycle. The PID and SMC controllers show saturation in the duty cycle most of the time, unlike the ZAD-FPIC controller, which leads to more stable switching frequency in the ZAD-FPIC technique.

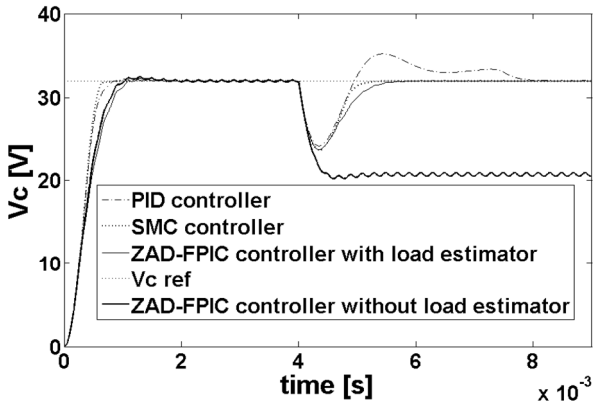

Figure 9. Behavior presented with load changes.

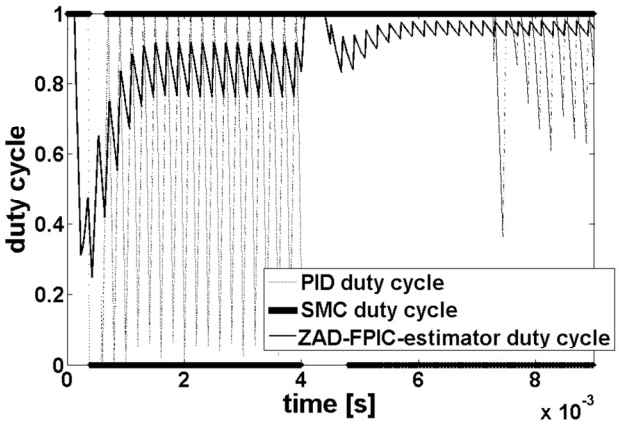

Figure 10. Duty cycle presented with load changes.

Figure (11) shows the numerical simulation including experimental limitations. Figures (12), (13), (14) and (15) show the experimental results, in this case the following

limitations are present: quantization effects A/D 12 bits and DPWM 9 bits, sampling frequency ($5\,kHz$) with 1 delay period, switching frequency ($5\,kHz$), ZAD-FPIC parameters are $Ks=4$ and $N=2$ and also the given in Table (1), PID parameters are $Ki=130415.7924$, $Kd=0.00644967$ and $Kp=59.80029$, SMC parameter is $c=Kp/(1.3*Kd)=8558.6109$. In discrete time the ZAD-FPIC control has better performance, PID and SMC has very high steady-state error.

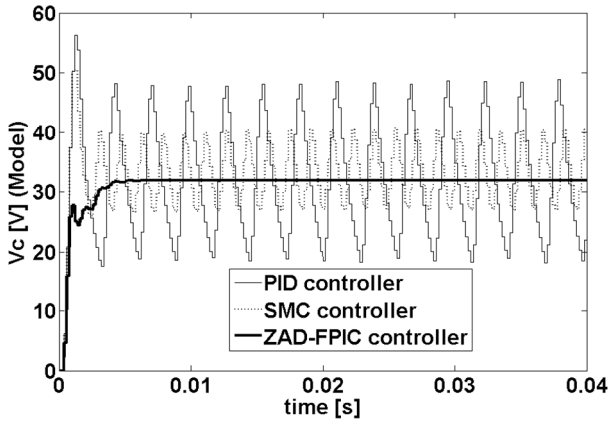

Figure 11. Numerical simulation with experimental limitations.

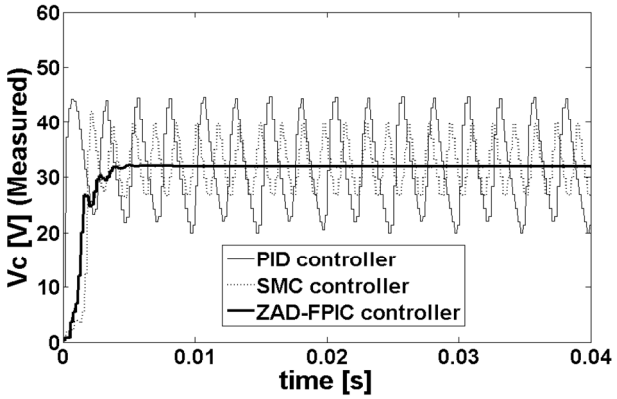

Figure 12. Experimental performance of controllers.

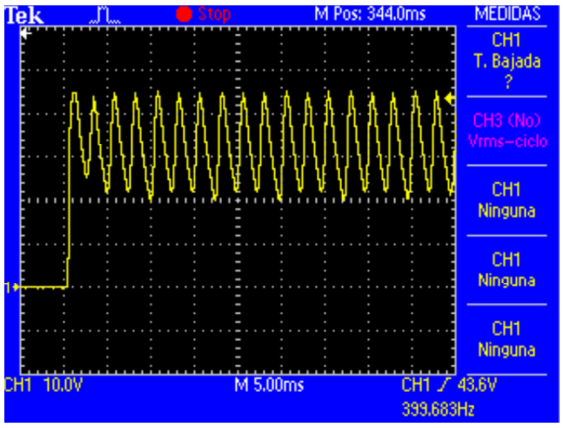

Figure 13. Experimental response for PID controller technique.

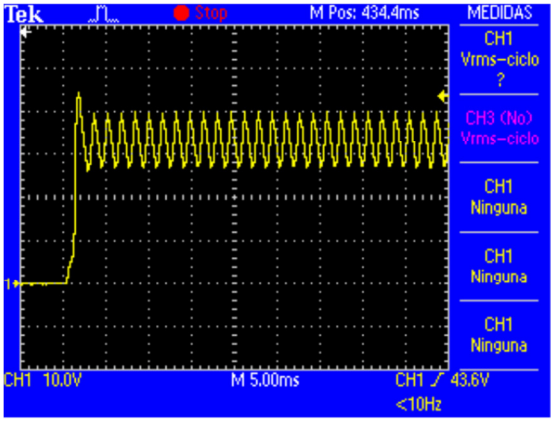

Figure 14. Experimental response for SMC controller technique.

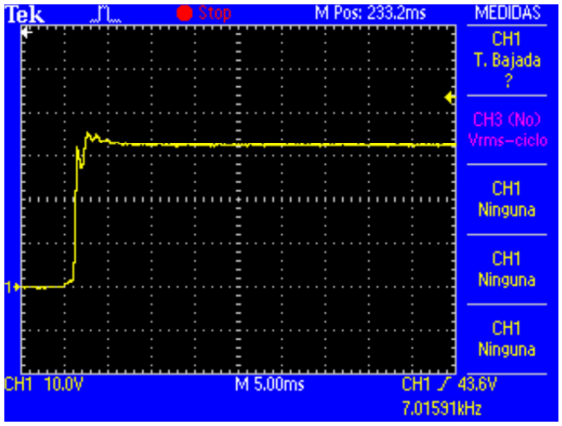

Figure 15. Experimental response for ZAD-FPIC-estimator controller technique.

V. CONCLUSIONS

The experimental results showed that the ZAD-FPIC techniques are better for the case where exist limitations such as: sampling, quantization and delay. For the continuous case all the controllers have good performance. When programming the controllers ZAD-FPIC is the most complicated. For the continuous case with load change, the

PID controller has more settling time, while the (ZAD-FPIC-without load estimator) does not regulate the output voltage. Through simulations and experiments it was observed that ZAD-FPIC controller has fixed switching frequency for the steady state case. The SMC and PID controllers work very well when devices with high sampling rates.

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