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Active inductor based fully integrated CMOS transmit/ receive switch for 2.4 GHz RF transceiver

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ABSTRACT

Modern Radio Frequency (RF) transceivers cannot be imagined without high-performance (Transmit/ Receive) T/R switch. Available T/R switches suffer mainly due to the lack of good trade-off among the performance parameters, where high isolation and low insertion loss are very essential. In this study, a T/R switch with high isolation and low insertion loss performance has been designed by using Silterra 0.13µm CMOS process for 2.4GHz ISM band RF transceivers. Transistor aspect ratio optimization, proper gate bias resistance, resistive body floating and active inductor-based parallel resonance techniques have been implemented to achieve better trade-off. The proposed T/R switch exhibits 0.85dB insertion loss and 45.17dB isolation in both transmit and receive modes. Moreover, it shows very competitive values of power handling capability (P1dB) and linearity (IIP3) which are 11.35dBm and 19.60dBm, respectively. Due to avoiding bulky inductor and capacitor, the proposed active inductor-based T/R switch became highly compact occupying only 0.003mm^2 of silicon space; which will further trim down the total cost of the transceiver. Therefore, the proposed active inductor-based T/R switch in 0.13µm CMOS process will be highly useful for the electronic industries where low-power, high-performance and compactness of devices are the crucial concerns.

Key words: active inductor, CMOS, ISM band, T/R switch, transceiver.

INTRODUCTION

The rapid development of modern compact wireless devices is driven by the fast growing market of wireless communication. Modern wireless transceivers essentially need an efficient T/R switch which serves the purpose of connecting either the receiver or transmitter to a common antenna, depending on control signals, to reduce the size and system cost, and offer device portability. It is one of the most crucial parts of a transceiver, which deals with both the high-power transmitter and low-power receiver circuit as shown in Fig. 1. During transmission phase, it connects the antenna to the power amplifier of the transmitter to radiate large signals to the surroundings and at the same time protects the low-power receiver circuit from being damaged (Kidwai et al. 2009, Bhuiyan et al. 2014b). On the other hand, during reception phase,

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it ensures that the low noise amplifier receives the intended signal with minimum loss.

Switches for RF devices can be implemented electronically using either integrated on-chip CMOS transistors or board-level components like GaAs, MESFETs, PIN diodes, or even MEMS (Li and Zhang 2010, Rosli et al. 2013). Conventionally, PIN diodes are given priority because of their moderate small signal performance and good linearity. But power dissipation and size are the important issues to be considered for PIN diodes (Chien et al. 2003). Besides, compound semiconductor switches such as GaAs have excellent impedance characteristics due to high electron mobility and high breakdown electric field to boost the power handling capability. Nevertheless, in these structures the presence of Schottky gates confines the forward bias voltage at the gate terminal to switch-on voltage of the Schottky diode which is about 0.7V for Silicon. It is, therefore, more complicated to fabricate a large number of MESFETs with smaller threshold voltages (Bakshi and Godse 2008). These problems necessitate the introduction of CMOS process to fabricate RF switch.

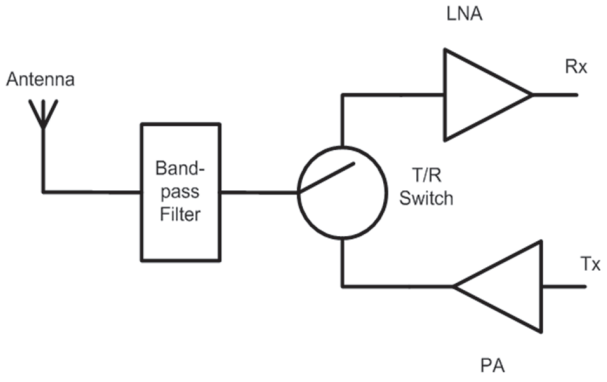

Figure 1 - T/R switch in RF transceiver front-end.

The rapid advancement of CMOS technology is making the circuits operated at RF regime feasible nowadays (Rebeiz and Muldavin 2001). Concurrent technologies allow the scientists to fabricate high-performance RFICs in laboratories as well as for commercial applications. Researchers, all over the world, are working to further enhance the performances of application-oriented RFICs by mitigating the CMOS problems at higher frequencies (Bhuiyan et al. 2014a, Li and Zhang 2010). Many researchers all over the world are adopting various techniques such as optimizing gate width of the transistors, DC biasing of the transistors, impedance transformation method, increasing the substrate impedance etc. to enhance their performances. Yamamoto et al. (2001) illustrated the basic concerns for better performance of a classic series-shunt type T/R switch which is nothing but the optimization of the gate width of the MOSs (Yamamoto et al. 2001). Although the design exhibited low isolation and low power handling capacity but because of using large CMOSs, the area of the total chip was large. For the further improvement in performance, Huang et al. (2001) introduced DC biasing of the transistors along with their proper optimization in the gate. This resulted in low insertion loss along with moderate isolation and power handling capacity (Huang et al. 2001). But he used relatively higher control voltages (6.0/2.0V) and the area of the layout was also reduced to a half, which is still large compared to concurrent CMOS switch circuits.

Huang (2004) and Hove et al. (2004) improved the isolation and insertion loss of the switch by utilizing impedance transformation and parasitic MOSFET model, respectively (Huang 2004, Hove et al. 2004). But power handling capacity of both the circuits was not adequate and the layout area of the switches was also large. In the same year, Talwalkar et al. (2004) adopted increased substrate impedance technique to offer a narrowband resonance, but with an increased chip area due to the usage of additional on-chip inductors (Talwalkar et al. 2004). Bhatti et al. (2005) introduced a transformer-based T/R switch only for low-power applications but with many complex matching requirements (Bhatti et al. 2005).

Yeh et al. (2006) utilized resistive body floating technique to improve the overall performance of the switch, but the power handling capacity and isolation of the switch were not adequate for high-power transceivers. Nevertheless, they reduced the size of the chip (Yeh et al. 2006). Mekanand et al. (2008) designed a switch by paralleling an NMOS and a PMOS instead of a single MOS to improve the dynamic range in the conducting state but the insertion loss of the switch was more than 1 dB (Mekanand et al. 2008). Liu et al. (2012) implemented the higher saturation voltage property of asymmetric transistors to improve the insertion loss and power handling capacity but the chip area of the switch was still quite high (Liu et al. 2012).

In this paper, proper optimization of transistors, resistive body floating, and parallel resonance techniques are used simultaneously to obtain high-performance series-shunt T/R switch at 2.4GHz ISM band in 0.13μm CMOS technology. At the same time, avoiding the usage of bulky inductors and capacitors in the circuit resulted in achieving very small chip size. Such a switch will be very useful for 2.4GHz ISM band RF transceivers for various applications.

T/R Switch Design Methodology

The proposed T/R switch circuit is shown in Fig. 2. Series-shunt topology is used in this design to achieve good isolation performance. The switching transistors (M1, M2) mainly perform the switching operation whereas the shunt arm transistors (M3 and M4), added at the transmitting and receive terminals, respectively, drain the unwanted leakage current to the ground. Two complement control signals, Vc and Vc′, are applied to the gate of the transistors to alternate the ON/OFF-states of the transistors. During the transmit mode, M1 is turned on to allow the signal to conduct from transmit port (TX) to the antenna (ANT); the off transistor M2 along with active inductor creates a high impedance path to the receiver terminal (RX) and M4 is turned on to form a low impendence path and direct the undesired signal at the receiver to the ground. Hence, the leakage signal is reduced and isolation is improved with a small degree of degraded insertion loss.

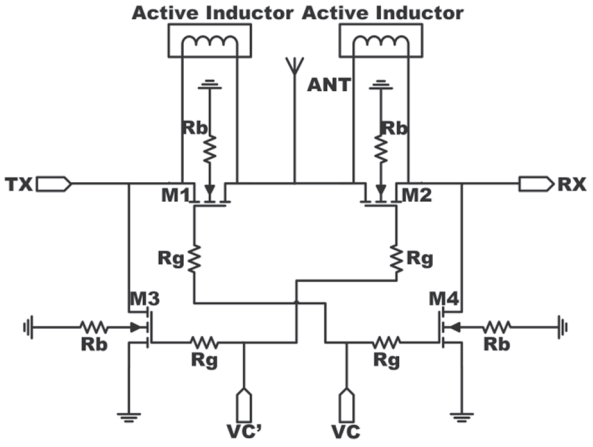

Figure 2 - Proposed T/R switch circuit.

In order to improve the performance of the switch, the following techniques are adopted in the basic circuit:

Transistor W/L optimization

The on-state resistance (R_{on}) of an MOS is given by (Zhang et al. 2006)

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \quad (1)$$

Where, μ_n is the mobility of electrons and C_{ox} represents capacitance per unit area of the gate.

Insertion loss is dominant by the on-state resistance of switching transistors. Equation (1) implies that R_{on} can be lowered by using transistors with high mobility, large (W/L) ratio, and high gate-to-source/channel voltage (V_{GS}). Therefore, NMOS transistors are used to realize the proposed switch because of their higher mobility. Besides, the NMOSs in the ON state are biased by 1.2V gate-to-channel voltage, which prevents both

avalanche and gate-oxide breakdown. In addition, (W/L) ratio of the MOSs is the prevailing factor that influences the ON resistance of transistor M2 and insertion loss as well. Therefore, insertion loss of the switch decreases with increase in W/L ratio of the transistor. But there is a limitation in the expansion of transistor width at higher frequencies. Because the source/drain to body parasitic capacitances play a vital role in degrading the isolation of the switch. In other words, there is an inevitable trade-off between R_{on} and parasitic capacitances, which results in an optimum value for the width of NMOSs at a given frequency band. For all the transistors in this design, minimum channel length has been chosen but the widths have been determined by trial and error basis. For each transistor, we varied the width until the best trade-off of parameters is achieved.

Resistive body floating

For improved power handling capacity, body floating technique is usually employed to cut down the signal loss through body junctions of the transistors (Yang et al. 2010). By conventional design, transistor body is usually attached directly to source or drain terminal and drain to source current is negligible under low input power, but at high-power level, the things become more critical. As input power increases, the diode between drain and body tends to turn on the extreme reversed bias on drain and source, which in turn results in lower input impendence of the transistor (Yeh et al. 2006). By connecting a large resistor (R_b) to the body of the transistor, high input impendence of the transistor is maintained and thus gives the switch better power performance, particularly in the wide-band frequency range.

Triple well NMOS

To handle high-voltage signals with usual MOS devices, device terminals are floated generally. In CMOS process, substrate floating may degrade the performance due to the low resistivity substrate (Lin et al. 2009). To solve the problem, triple-well NMOS devices are used in this design. In such a structure, P-well of the transistor is embedded within a deep N-well to create an isolated body from the P-substrate as shown in Fig. 3 (Han et al. 2008, Kim et al. 2010). This detaches the body from the substrate and offers to bias the body of the transistor and deep N-well separately. Thus, design robustness is improved (Heifeng and O 2007).

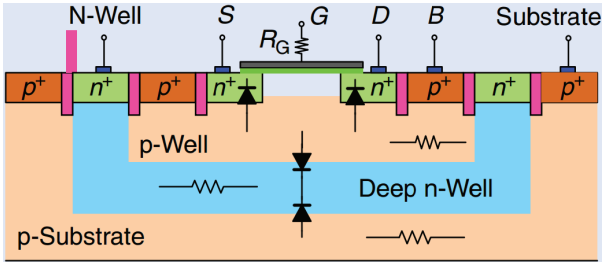

Figure 3 - Triple well NMOS transistor structure. (See the colors in the online version).

Gate bias resistor

Gate bias resistor (R_g) is added to the transistor gate to provide better DC bias isolation and enhance the power handling capacity further. This technique also stabilizes V_{gd} and V_{gs} of the transistor and improves the linearity (Mekanand et al. 2008). These resistances are also used to mitigate the voltage fluctuations around the gate terminal, which can affect the channel resistance as well as cause breakdown at the gate terminal (Qiang and Zhang 2007). Moreover, suitable gate bias resistor is very important to maintain the switching speed of the transistor.

Active inductor based parallel resonant circuit

Isolation is good at low frequencies due to the high off-state resistance but degrades significantly at high frequency as the signal couples through the off state capacitance (Huang et al. 2001).

The addition of an inductor across the switching transistor creates an LC tank circuit which ex-

hibits virtually infinite impendence at the resonance frequency. This helps to reduce the leakage signal during resonance and results great improvement in isolation. In previous research, the on-chip spiral inductor has already been used to implement parallel resonance technique (Yang et al. 2010). However, the on-chip spiral inductor has a low-quality factor (Q), low inductance value and occupies a larger area. A floating active inductor with resistive feedback, as shown in Fig. 4 (Tao and Fa 2010), has been used in design to replace on-chip spiral inductor in order to achieve higher Q while maintaining small chip size. The active inductor is based on a gyrator-C concept where M7 and M8 are in common source configuration. M9, M10 serve as a bias current source and M5, M6 used as cross-coupled transconductance stage. The Q factor and inductance are increased by the feedback resistor added across the cross-coupled pair (Tao and Fa 2010).

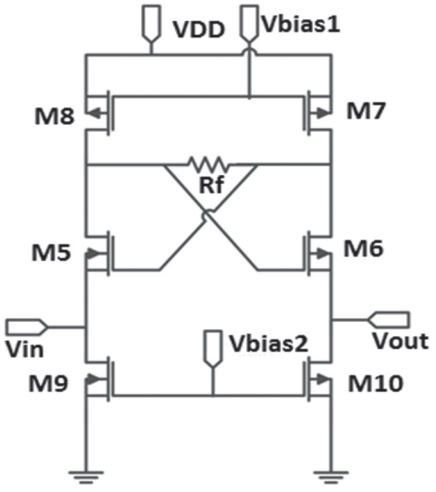

Figure 4 - Floating active inductor (Tao and Fa 2010).

Table I and Table II give the specifications of the components used in the proposed design.

RESULTS AND DISCUSSION

The proposed active inductor-based T/R switch is designed and simulated in Silterra 0.13µm CMOS process. Design-Architect (DA-IC) and IC station tools of Mentor Graphics environment have been used for this simulation. In this research, all the performance parameters like insertion loss, isolation, linearity, power handling capacity, stability etc. of the switch are evaluated. Moreover, statistical analyzes are also performed to verify the reliability of the switch.

TABLE I
Circuit parameter for series shunt T/R switch.

Label	Type	Parameters
M1, M2	NMOS	W/L = 100µm/ 0.13µm
M3, M4	NMOS	W/L = 40µm/ 0.13µm
Rb, Rg	Resistor	Resistance = 10K

TABLE II
Circuit parameter for active Inductor.

Label	Type	Parameter
M5, M6	NMOS	W/L = 15µm/ 0.13µm
M7, M8	PMOS	W/L = 25µm/ 0.13µm
M9, M10	NMOS	W/L = 10µm/ 0.13µm
Rf	Resistor	Resistance = 10K
Vbias1	Voltage source	Voltage = 0.3V
Vbias2	Voltage source	Voltage = 0.7V

Fig. 5 shows the insertion loss and isolation performance of the switch against the input signal frequency. From the figure, it is clear that the insertion loss is degraded at higher frequencies which is mainly due to the influence of junction capacitance of the MOSs. On the other hand, isolation of the switch is found to increase and reach a maximum at the resonant frequency of 2.4GHz set by the active inductor and capacitance of the non-conducting switching transistor, then again its value is degraded as the frequency increases. The leakage through the active inductor circuit at frequencies other than the resonant frequency causes degradation of its isolation performance. The insertion loss and isolation of the proposed switch at 2.4GHz are 0.85dB and 45.17dB respectively, for both transmit and receive modes of operation. The results are same for both transmit and receive modes due to symmetrical schematic design.

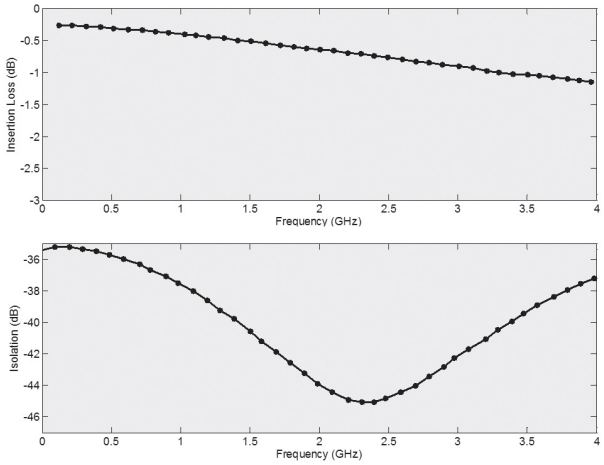

Figure 5 - Insertion loss and isolation performance of the switch.

A power compression point of 1dB (P1dB) basically measures the linearity and power handling capacity of a circuit. Operating at the power level beyond this point will result in the nonlinear behavior and causes harmonic distortion to the signal. Fig. 6 shows the large signal linearity of the switch and the value of the P1dB obtained is 11.35dBm. In two tones analysis, the fundamental and third intermodulation power curves intercept at an input power of 19.60dBm, as shown in Fig. 7, which is its IP3 value. It indicates when the amplitude of the third-order products equals the input signals.

Statistical analysis is very important in the absence of measured results. The FEOL corner and Monte Carlo analyzes of the proposed switch is shown in Fig. 8 and Fig. 9. The insertion loss is found better for FF corner and get worse in SS corner. On the other hand, the isolation is the best in FF corner and worse in SS corner. In both cases, the mean deviation from TT for both corners is consistent. As all transistors or resistors used are large and therefore, a small conductivity variation does not affect the switch parameters strongly. In Monte Carlo analysis, for 50 runs or counts, the insertion loss was within the range between 0.88dB and 0.83dB, whereas isolation was within 44.8dB and 45.4dB. The results showed that the performance parameters of the switch were stable within the acceptable range.

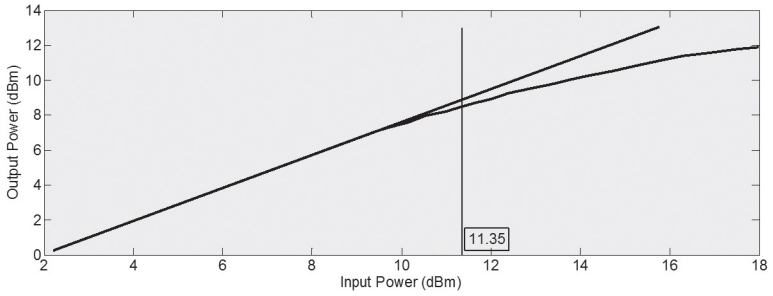

Figure 6 - Power handling performance of the switch.

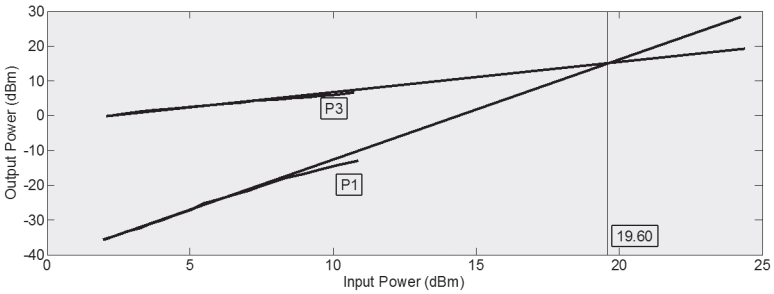

Figure 7 - Linearity of the switch.

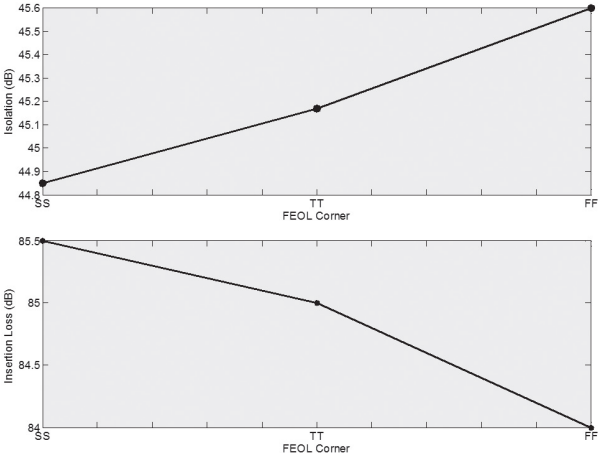

Figure 8 - FEOL Corner analysis.

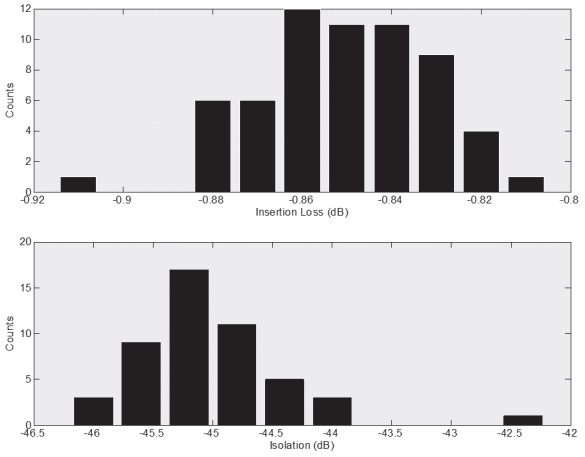

Figure 9 - Monte Carlo analysis.

Fig. 10 shows the complete layout of the proposed switch. In this design, triple-well isolated MOSFET structure with body floating technique has been used. Multi-finger structure has also been implemented for transistors with large aspect ratios to keep the conductivity within the certain acceptable value. The dimension of the switch is only 0.003mm^2.

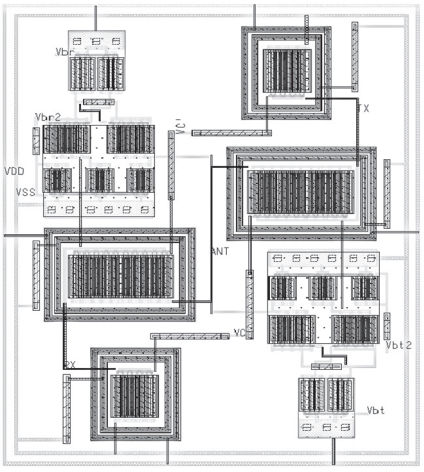

Figure 10 - Core layout design of the proposed switch with area 0.003mm^2.

The major improvement in this T/R switch is the isolation and insertion loss at a very small die area. Optimum isolation performance at the 2.4GHz is obtained by introducing active inductor-based parallel resonance circuit. Moreover, usage of the adequate aspect ratio of the switching and shunt transistors helps the switch to achieve low insertion loss. High isolation is essential to stop power leaking to the receiver to retain the transmission efficiency and also for protecting the low-power receiver circuit during the transmit mode. Whereas the low insertion loss ensures that the antenna receives maximum power to radiate. On the other hand, low insertion loss and high isolation are vital for reception mode because the receiver receives very weak signal and the leakage toward the transmitter will further weaken the signal. The high insertion loss degrades the receiver output whereas low isolation demeans the noise figure of the receiver. Both the parameters are directly related to efficiency and performance of the transceiver. Another attractive feature is that the switch can be easily redesigned for other operating frequencies due to the tunable inductance value of the active inductor. Therefore, the proposed switch with 45.17dB isolation and 0.85dB insertion loss can be a good choice for low-power compact RF transceivers.

A comparison of this work to the recently reported performances of 2.4GHz CMOS switches is given in Table III. In (Zhang et al. 2006), fully differential architecture is used to improve

TABLE III
Comparison of T/R switch performance.

Reference	CMOS Technology	IL (dB)	ISO (dB)	P1dB (dBm)	Chip Size (mm^2)
(Zhang et al. 2006)	0.18µm	1.3	20	15	0.024
(Yeh et al. 2006)	0.18µm	0.7	35	21	0.03
(Heifeng and O 2007)	0.13µm	0.8	31	28	0.09
(Han et al. 2008)	65nm	0.8	28	30.8	0.20
(Lin et al. 2009)	0.18µm	0.94	28.4	30	2.25
(Kim et al. 2010)	0.18µm	0.5	23	33.8	0.203
(Liu et al. 2012)	0.18µm	0.62	33	29.2	0.125
(Tan et al. 2012)	32nm	1.3	32	34	-
(Chen and Lin 2014)	0.18µm	0.72	24.5	22.4	0.037
This work	0.13µm	0.85	**45.1**	11.35	**0.003**

the linearity while keeping the chip area small. The switch occupied very small chip size and exhibit adequate power handling capability but the isolation performance is poor compared to others. A multi-section impedance transformation technique is adopted to realize a high-power differential switch but the isolation of the switch is poor compared to other designs (Tan et al. 2012). A different approach to layout design was taken in (Yeh et al. 2006) to improve the performance by reducing high-frequency substrate coupling and substrate loss. Although the power performance of the design was improved but the insertion loss of the switch was very high. Asymmetrical transistor structure was used to design series-shunt switch in (Liu et al. 2012). The switch had a very low insertion loss and high power handling capability but the die area of the total chip was still large. Use of high resistivity substrate along with stacked transistor arrangement made it possible to attain high isolation with moderate P1dB but at the cost of comparatively large chip area. However, our proposed design achieved the highest isolation and lowest chip area compared to the previous researches. Besides, power handling capability has a competitive value and meets a certain range of RF application requirements. Furthermore, the chip area of the design is the lowest compared to the previous researches.

CONCLUSIONS

High-performance and fully integrated SPDT T/R switch is one of the major requirements of every modern RF device. In this study, a high-performance fully on-chip 2.4GHz T/R switch in 0.13µm CMOS technology has been illustrated. The results exhibit 0.85dB insertion loss, 45.17dB isolation, and 11.35dBm power handling capacity in both transmit and receive mode, with 1.2/0V control voltages. The body-floating technique, proper transistor optimization, triple-well-structured transistor and parallel resonance with active inductor made the proposed switch attaining low insertion loss, high isolation, faster-switching speed, good power performance, and linearity simultaneously. Besides, the chip area of the switch is reduced drastically with the elimination of bulky inductors and capacitors in the design. It occupies only $0.003mm^2$ and it is the lowest ever reported in this frequency band. Moreover, the stability and reliability of the switch make it very much suitable for 2.4GHz wireless terminals.

ACKNOWLEDGMENTS

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RESUMO

Não se pode imaginar transmissões modernas por radiofrequência (RF) sem o uso de um comutador T/R (*Transmit/Receive switch*) de alto desempenho. As opções para estes dispositivos ora disponíveis podem ser penalizadas pelo compromisso de escolha entre os parâmetros para avaliação de desempenho, onde um alto isolamento e baixa perda por inserção do dispositivo são ambos essenciais. Neste estudo, um comutador T/R com alto isolamento e baixa perda de inserção foi projetado, utilizando processo CMOS de 0,13μm da SilTerra para transceptores com banda de radiofrequência de 2,4 GHz ISM (banda Industrial, Científica e Médica). Para se obter um melhor compromisso, implementou-se: uma razão de aspecto otimizada para os transistores; reistência apropriada para polarização de porta; corpo flutuante resistivo e técnicas de ressonância paralela baseadas em indutor ativo. O comutador T/R proposto possui perda por inserção de 0,85 dB e isolamento de 45,17 dB, seja no modo de transmissão ou de recepção. Em adição, o dispositivo apresenta valores competitivos de potência disponível (P1dB) e linearidade (IIP3), que são de 11,35 dBm e 19,60 dBm, respectivamente. Evitando-se a utilização dos volumosos indutores e capacitores usuais o comutador T/R resultante, baseado em indutor ativo, mostrou-se muito compacto, ocupando apenas 0,003 milímetros quadrados de espaço de silício, o que contribui para a redução de custos de fabricação. Dessa forma, o comutador proposto baseado em indutor ativo construído por processo CMOS 0,13μm será muito útil para indústrias eletrônicas, onde baixa potência, alto desempenho e redução de volumes de dispositivos são questões cruciais.

Palavras-chave: indutor ativo, CMOS, banda ISM, comutador T/R, transceptor.

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