Ciência e Natura
ISSN: 0100-8307
cienciaenaturarevista@gmail.com
Universidade Federal de Santa Maria
Brasil

Abbasi Morad, Milad Jalalian; Reza Talebiyan, Seyyed; Pakniyat, Ebrahim
Design of New High-Performance Full Adder Using Hybrid-CMOS Logic Style for High-Speed Applications
Ciência e Natura, vol. 37, núm. 6-2, 2015, pp. 285-290
Universidade Federal de Santa Maria
Santa Maria, Brasil

Ciência e Natura, v. 37 Part 2 2015, p. 285–290

ISSN impressa: 0100-8307 ISSN on-line: 2179-460X

Design of New High-Performance Full Adder Using Hybrid-CMOS Logic Style for High-Speed Applications

Milad Jalalian Abbasi Morad [1], Seyyed Reza Talebiyan [2] and Ebrahim Pakniyat [3]

[1]Department of Electrical Engineering, Imam Reza International University, Mashhad, Iran
[2]Department of Electrical Engineering, Imam Reza International University, Mashhad, Iran
[3]Department of Electrical Engineering, Imam Reza International University, Mashhad, Iran

Abstract

This paper, presents a new design for 1-bit full adder cell using hybrid-CMOS logic style. Using a novel structure for implementation of the proposed full adder caused it has better performance in terms of propagation delay and power-delay product (PDP) compared to its counterparts. According to the simulation results, the propagation delay of the proposed full adder is 22.8% less than the propagation delay of next fastest full adder, and the power-delay product of the proposed full adder is 22.7% less than the next best PDP. HSpice simulations using 65nm technology with a power supply of 1.2V was utilized to evaluate the performance of the circuits.

Keywords*: full adder, high-performance, high-speed, hybrid-CMOS, propagation delay.*

Recebido: dia/mês/ano Aceito: dia/mês/ano

1 Introduction

Most of the VLSI applications, such as digital signal processing, image and video processing, and digital filter design, widely use arithmetic operations. Addition, subtraction and multiplication are examples of the most commonly used operations. The 1-bit full adder cell is the building block of these units. Hence, improving its performance is critical for improving the overall unit performance. The most important performance parameters for a generic VLSI system are power consumption, speed, and chip area. Several logic styles have been used in the past to design full adder cells. Each logic style has its own advantages and disadvantages. Classical designs of full adders normally used only one logic style for the whole full adder design. Standard static CMOS, members of pass-transistor logic (PTL) family such as CPL, DPL, SRPL, and transmission gate are the most important logic styles in the conventional full adders (Zimmermann & Fichtner, 1997). In the other full adder designs, more than one logic style have been used. These designs are called hybrid-CMOS logic style (Zavarei, Baghbanmanesh, Kargaran, Nabovati, & Golmakani, 2011). These designs use the features of different logic styles to improve upon the performance of the designs using single logic style. HPSC full adder (hybrid pass logic with static CMOS output drive full adder) (Zhang, Gu, & Chang, 2003), New-HPSC adder (Chang, Gu, & Zhang, 2005), New-Hybrid-CMOS adder (Goel, Kumar, & Bayoumi, 2006), and full adders proposed in (Zavarei et al., 2011), (Musala & Reddy, 2013), (Lin, Hwang, & Sheu, 2012) and (Agarwal, Agrawal, & Alam, 2014), are the examples of adders designed with this logic style. In this paper, a novel 1-bit full adder has been proposed with better performance in comparison with New-HPSC, New-Hybrid-CMOS adders, and full adders proposed in (Zavarei et al., 2011), (Musala & Reddy, 2013), (Lin et al., 2012) and (Agarwal et al., 2014). Some of them are shown in Figure 1.

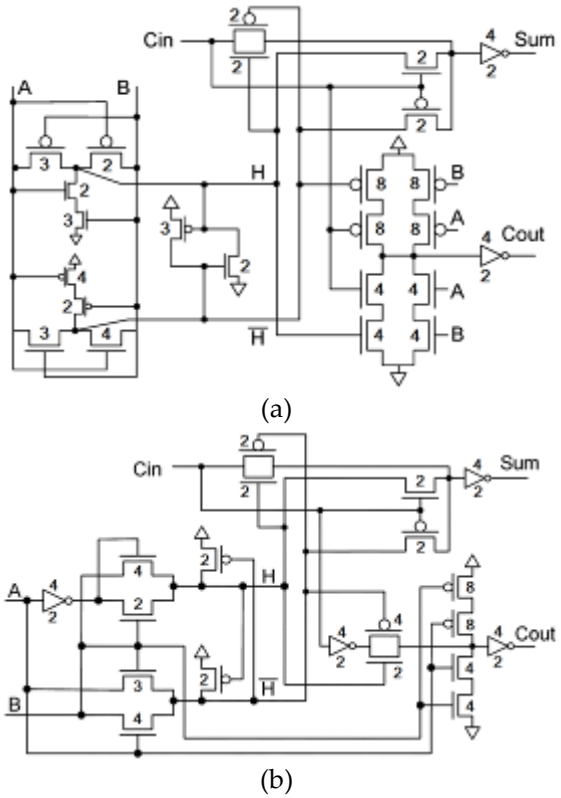

Figure 1: Standard existing full adder cells, (a) New-HPSC and (b) New-Hybrid-CMOS.

The rest of this paper is organized as follow, in section 2, the main structure of a 1-bit full adder will be introduced. Then in section 3, the two new 1-bit full adder cells will be proposed. In section 4, simulation environment will be described and in section 5 simulation results will be expressed, which show the supremacy of the proposed cells. Finally, in section 6, this paper will be concluded.

2 Main structure of 1-bit full adder

Generally, hybrid-CMOS full adders are categorized in three groups depending on their structure and logical expression of Sum output (Goel et al., 2006). The first category of full adders is based on XOR gates (XOR-XOR based full adder) and second one is based on XNOR gates (XNOR-XNOR based full adder). In third category, the Sum and Carry outputs are generated by XOR-XNOR intermediate signals (Zavarei et al., 2011) (centralized full adder). In

Recebido: dia/mês/ano Aceito: dia/mês/ano

this paper, the proposed full adder stand on third category.

The Sum and Carry (Cout) outputs of a 1-bit full adder generated from the binary inputs A, B, and Cin can be generally expressed as

$$SUM = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = A.B + C_{in}\left(A \oplus B\right) \quad (2)$$

In third category, the Sum and Carry outputs are generated by the following expression, where H is the XOR of A and B, and H′ is the complement of H.

$$\begin{aligned} SUM &= H \oplus C_{in} \\ &= H.C'_{in} + H'.C_{in} \end{aligned} \quad (3)$$

$$C_{out} = B.H' + C_{in}.H \quad (4)$$

Generally, this category is divided by three modules. Module-1 is an XOR-XNOR circuit producing H and H′ signals. Module-2 and 3 produce Sum and Cout as outputs, respectively. Module-2 and 3 are 2-to-1 multiplexers with H and H′ as select lines.

The general form of this category is shown in Figure 2 (Goel et al., 2006).

The simultaneous generation of H and H′ signals is critical in these types of adders, because they drive the select lines of the multiplexers in the output stage. Otherwise, there may be glitches and unnecessary power dissipation may be occur (Zavarei et al., 2011).

3 Proposed full adder

As The main structure of 1-bit full adder introduced in section 2. As mentioned in the previous section, the proposed full adder stands on third category. This is shown in Figure 3. The intermediate signals H and H′ are produced by module-1 which has been implemented by a novel structure.

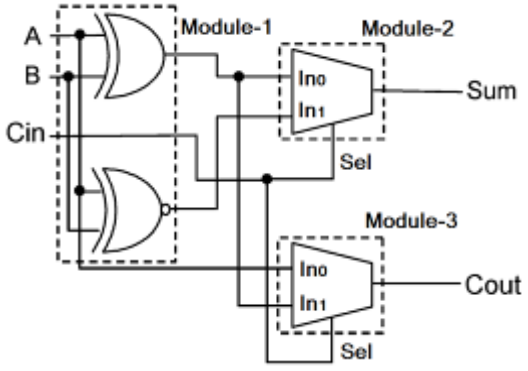

Figure 2: General form of centralized full adder.

Module-2 is a multiplexer that acts as an XOR gate and generates Sum as output. Module-3 is a multiplexer with H and H′ as select lines, and produces the Carry output signal.

4 Description of simulation environement

HSpice simulations using 65nm technology with a power supply of 1.2V was utilized to evaluate the performance of the seven circuits. To simulate a real environment, input buffers for all inputs of the test circuit are used. The transistor sizes of these buffers are chosen such that there is sufficient signal distortion as expected in an actual circuit. A minimum output load of fan-out of four inverters (FO4) is used for power and delay measurements (Goel et al., 2006), the value of which amounts to 1.234fF (about 0.308fF for each inverter in 65nm technology). The generic simulation test bench used is shown in Figure 4 along with the transistor sizes of each buffer (Zavarei et al., 2011). To reach more accurate results, all transitions from an input combination to another (56 patterns) have been tested, and the delay at each transition has been measured. The maximum has been reported as the cell delay. Figure 5 shows the output signals and input stimulus used for the full adder circuits.

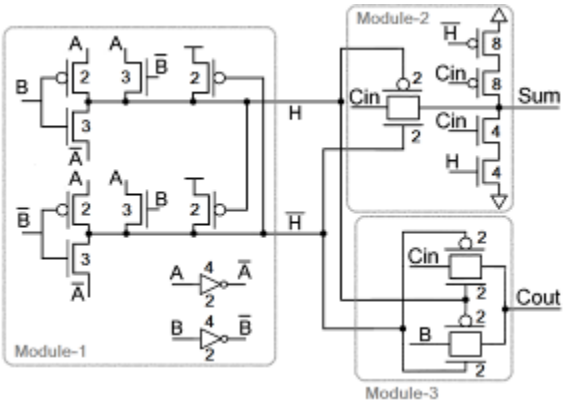

Figure 3: Proposed full adder.

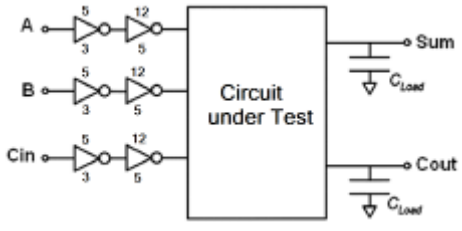

Figure 4: Simulation test bench.

Recebido: dia/mês/ano Aceito: dia/mês/ano

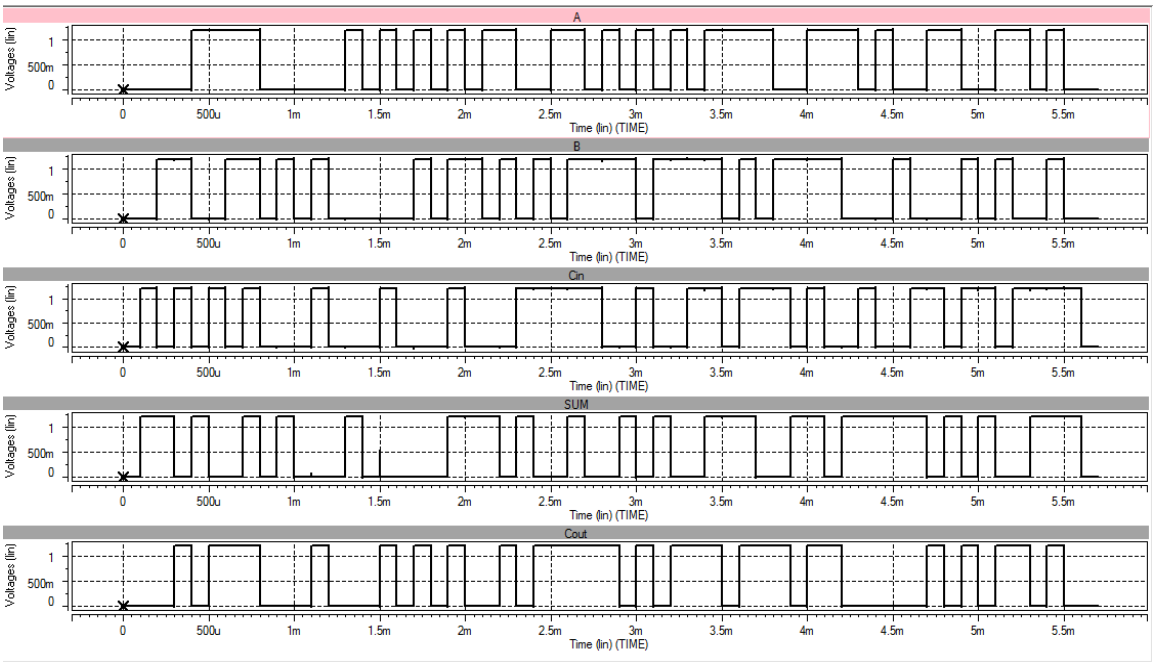

Figure 5: Output signals and input stimulus used for the full adder circuits.

The average power for the duration of this pattern has been reported as the cell power consumption figure. In order to have a fair comparison, all the simulated circuits are prototyped at optimum transistor sizing. The transistor sizes of all the simulated circuits have been included in the figures. In the circuits, the numbers depict the width (W) of the transistors with the minimum feature size as 2λ. All the circuits have been sized to achieve best PDP. For the calculation of power-delay product, worst-case delay is chosen to be larger delay amongst the two outputs.

5 Simulation results

In this section, simulation of the full adder cells is presented under the mentioned conditions in previous section. The circuit performance of the test circuits is evaluated in terms of worst-case delay, power dissipation, and power-delay product at 1.2V supply voltage. The simulation results are shown in Table 1. According to the results, the proposed full adder is the best structure in terms of propagation delay and power-delay product (PDP). The propagation delay of the proposed full adder is 23% less than the propagation delay of next fastest full adder (New-HPSC). The power-delay product (PDP) of the proposed full adder is 23% less than the next best PDP (PDP for FA in (Musala & Reddy, 2013)). The PDP and delay improvements of the proposed full adder are shown in Table 2.

Table 1: Simulation results for the full adders

FA	Power (nW)	Delay (pS)	PDP (e-18)
New HPSC	2.01	136.52	0.275
New Hybrid CMOS	1.96	151.51	0.297
FA in (Zavarei et al., 2011)	2.09	142.85	0.298
FA in (Musala & Reddy, 2013)	1.90	138.62	0.264
FA in (Lin et al., 2012)	2.15	550.48	1.18
FA in (Agarwal et al., 2014)	1.79	257.28	0.461
Proposed	1.94	105.35	0.204

Table 2: Improvements of the Proposed Adder

FA	Delay improvement of the proposed FA	PDP improvement of the proposed FA
New HPSC	23%	26%
New Hybrid CMOS	30%	31%
FA in (Zavarei et al., 2011)	26%	32%
FA in (Musala & Reddy, 2013)	24%	23%
FA in (Lin et al., 2012)	81%	83%
FA in (Agarwal et al., 2014)	59%	56%

Recebido: dia/mês/ano Aceito: dia/mês/ano

The simulation results for power consumption, propagation delay and PDP have been depicted in Figures 6 to 8.

Different loading conditions are also considered to evaluate the performance of the test circuits (1.234-30 fF) in terms of power consumption, delay and PDP. Load of 30fF is roughly equal to the input load capacitance of one hundred CMOS inverter gates. The values of power consumption, delay and PDP for different loading conditions are shown in Figures 9 to 11.

As can be seen, the proposed full adder is the best structure in terms of delay and PDP at all output load conditions, and, therefore, it has the best drivability compared to its counterparts.

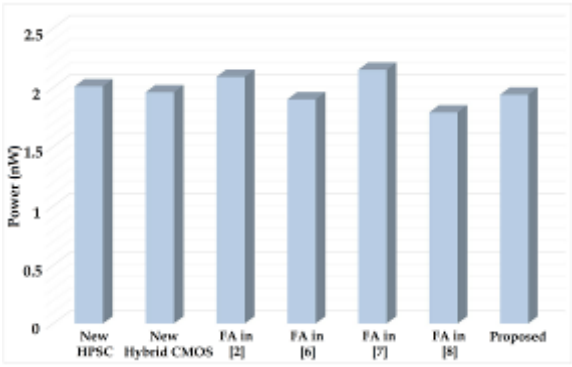

Figure 6: Power consumption results for different full adders.

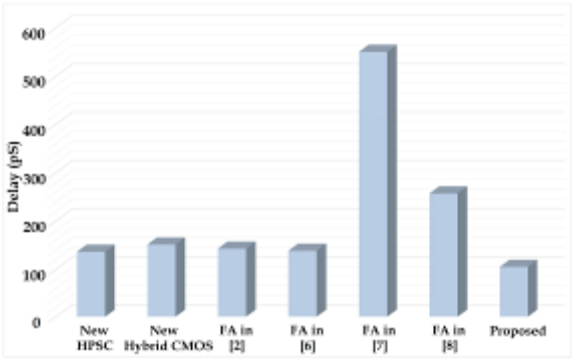

Figure 7: Propagation delay results for different full adders.

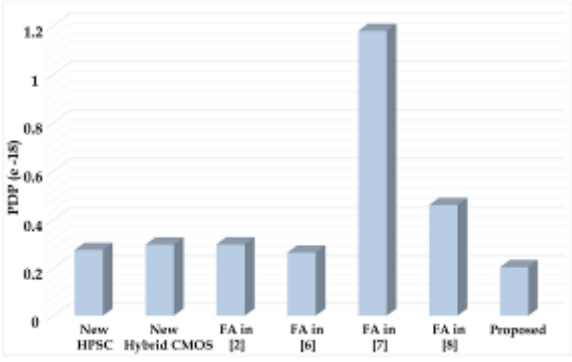

Figure 8: PDP results for different full adders.

6 Conclusions

A novel 1-bit full adder has been proposed. The proposed full adder has the best performance in terms of delay and PDP compared to other full adders.

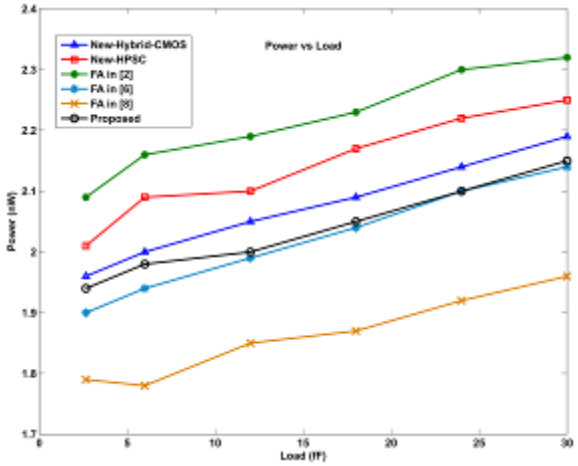

Figure 9: Power consumption results under different load conditions.

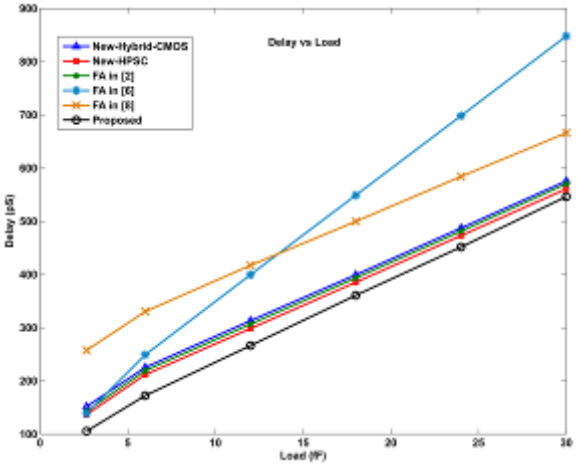

Figure 10: Delay results under different load conditions.

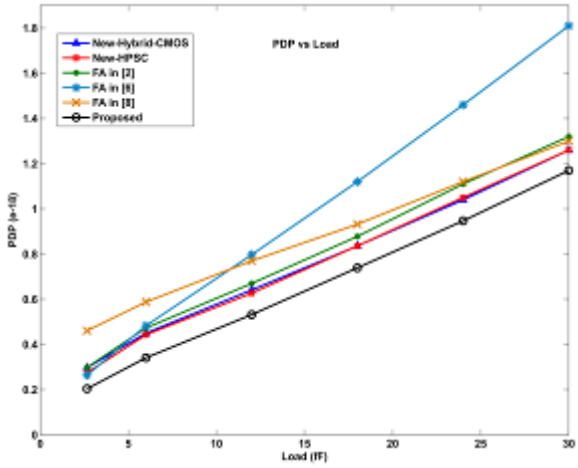

Figure 11: PDP results under different load conditions.

Recebido: dia/mês/ano Aceito: dia/mês/ano

The simulation results indicated that the proposed full adder has minimum PDP under different load conditions compared to its counterparts and, therefore, it has the best drivability. Since the performance of the proposed full adder is good, it can embed as a multi-bit full adder.

References

Agarwal, M., Agrawal, N., & Alam, M. (2014). A new design of low power high speed hybrid CMOS full adder. Paper presented at the Signal Processing and Integrated Networks (SPIN), 2014 International Conference on.

Chang, C.-H., Gu, J., & Zhang, M. (2005). A review of 0.18-/spl mu/m full adder performances for tree structured arithmetic circuits. Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, 13(6), 686-695.

Goel, S., Kumar, A., & Bayoumi, M. (2006). Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style. Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, 14(12), 1309-1321.

Lin, J.-F., Hwang, Y.-T., & Sheu, M.-H. (2012). Low power 10-transistor full adder design based on degenerate pass transistor logic. Paper presented at the Circuits and Systems (ISCAS), 2012 IEEE International Symposium on.

Musala, S., & Reddy, B. R. (2013). Implementation of a full adder circuit with new full swing EX-OR/EX-NOR gate. Paper presented at the Microelectronics and Electronics (PrimeAsia), 2013 IEEE Asia Pacific Conference on Postgraduate Research in.

Zavarei, M. J., Baghbanmanesh, M. R., Kargaran, E., Nabovati, H., & Golmakani, A. (2011). Design of new full adder cell using hybrid-CMOS logic style. Paper presented at the Electronics, Circuits and Systems (ICECS), 2011 18th IEEE International Conference on.

Zhang, M., Gu, J., & Chang, C.-H. (2003). A novel hybrid pass logic with static CMOS output drive full-adder cell. Paper presented at the Circuits and Systems, 2003. ISCAS'03. Proceedings of the 2003 International Symposium on.

Zimmermann, R., & Fichtner, W. (1997). Low-power logic styles: CMOS versus pass-transistor logic. Solid-State Circuits, IEEE Journal of, 32(7), 1079-1090.

Recebido: dia/mês/ano Aceito: dia/mês/ano