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# Selection of MOSFET Sizes by Fuzzy Sets Intersection in the Feasible Solutions Space

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## ABSTRACT

A fuzzy sets intersection procedure to select the optimum sizes of analog circuits composed of metal-oxide-semiconductor field-effect-transistors (MOSFETs), is presented. The cases of study are voltage followers (VFs) and a current-feedback operational amplifier (CFOA), where the width ( $W$ ) and length ( $L$ ) of the MOSFETs are selected from the space of feasible solutions computed by swarm or evolutionary algorithms. The evaluation of three objectives, namely: gain, bandwidth and power consumption; is performed using HSPICE<sup>TM</sup> with standard integrated circuit (IC) technology of 0.35 $\mu$ m for the VFs and 180nm for the CFOA. Therefore, the intersection procedure among three fuzzy sets representing "gain close to unity", "high bandwidth" and "minimum power consumption", is presented. The main advantage relies on its usefulness to select feasible  $W/L$  sizes automatically but by considering deviation percentages from the desired target specifications. Basically, assigning a threshold to each fuzzy set does it. As a result, the proposed approach selects the best feasible sizes solutions to guarantee and to enhance the performances of the ICs in analog signal processing applications.

Keywords: Fuzzy sets, fuzzy set intersection, circuit sizing, analog circuits, MOSFET, evolutionary algorithms.

## RESUMEN

Se presenta un procedimiento basado en la intersección de conjuntos difusos para la selección de las dimensiones óptimas de circuitos analógicos compuestos por transistores de efecto de campo metal-óxido-semiconductor (MOSFETs). Los casos de estudio son seguidores de voltaje (VFs) y un amplificador operacional retroalimentado en corriente (CFOA), donde el ancho ( $W$ ) y el largo ( $L$ ) de los MOSFETs son seleccionados desde el espacio de soluciones factibles calculadas por algoritmos evolutivos o de partículas. La evaluación de tres objetivos, que representan: ganancia, ancho de banda y consumo de potencia; se realiza utilizando HSPICE<sup>TM</sup> con tecnología estándar de circuitos integrados de 0.35 $\mu$ m para el caso de los VFs, y 180nm para el CFOA. Por lo tanto, se presenta el procedimiento de intersección de tres conjuntos difusos los cuales representan la "ganancia cercana a la unidad", el "ancho de banda alto" y "mínimo consumo de potencia". La ventaja principal es su utilidad para seleccionar dimensiones  $W/L$  factibles automáticamente, pero el procedimiento toma en cuenta porcentajes de desviación con respecto a las especificaciones deseadas. Básicamente, esto se hace mediante la asignación de un valor de umbral para cada conjunto difuso. Como resultado, la aproximación propuesta selecciona la mejor solución factible para garantizar y mejorar el desempeño de CIs en aplicaciones de procesamiento de señales analógicas.

## 1. Introduction

Analog integrated circuit (IC) design using metal-oxide-semiconductor field-effect-transistors (MOSFETs) imposes challenges in sizing and selecting the right circuit topology [1,2], because a huge plethora of active devices exist [3,4]. The sizing problem is related to finding the optimal width and length ( $W/L$ ) values of the MOSFETs to guarantee optimal performance of active filters,

oscillators, sensor conditioning circuits and so on [5, 6, 7, 8, 9, 10, 11]. The problem on choosing the right circuit topology is known as circuit synthesis [1, 2, 12, 13, 14, 15], and it is accompanied of a sizing procedure. In that case, the selected topology must accomplish a specific function which best behavior is performed by the appropriate ( $W/L$ ) sizing of its circuit elements.

For instance, among all kinds of active devices [1, 2, 3, 4], this work pays attention to unity-gain cells (UGCs), not only because of their usefulness to evolve for the creation of more complex analog circuits [14], but also because they are quite useful in implementing linear [1,2] and nonlinear [16, 17, 18] circuit applications. Henceforth, this work shows a fuzzy-sets-intersection approach to select the optimum  $W/L$  sizes of three voltage followers, from an space of feasible solutions which can be computed by metaheuristics [19], swarm [20, 21, 22] or evolutionary algorithms [23, 24, 25, 26]. To highlight the usefulness of the proposed approach, it is also applied to a bigger active device known as current-feedback operational amplifier (CFOA) [14, 15].

Fuzzy sets and fuzzy logic have been applied successfully in electronics [27, 28], and also in the analog IC design automation process [29, 30, 31]. Basically, their usefulness is exploited to handle uncertainties, to capture human expertise and to drive subjective ideas such as “high”, “close to”, “low”, etc. In the following, an intersection procedure among three fuzzy sets representing fuzzy variables such as “gain close to unity”, “high bandwidth” and “minimum power consumption”, is described.

## 2. Fuzzy Sets Intersection

Among the four UGCs [14], the ideal voltage follower (VF) provides unity-gain, infinity bandwidth (BW) and zero power consumption (PC). When sizing the VF, the gain is close to unity, the BW and PC are finite, and other performance parameters are also affected. Fuzzy sets are well suited to represent these real behaviors under several parameter values, depending on the  $W/L$  ratios of the MOSFETs, voltage and current bias levels, and load capacitor. Therefore, as fuzzy sets allow formalizing linguistic sentences to express subjective ideas which can be interpreted in different ways by various individuals, one can define appropriate membership functions in order to construct three fuzzy sets to represent: high BWs, gain closer to unity and low PC.

The intersection of such fuzzy sets provides the sizes that satisfy the three fuzzy conditions. In addition, by including a percentage variation

(threshold) one obtains feasible  $W/L$  sizes accomplishing desired target characteristics around that threshold, so that an analog IC designer can select the more appropriated  $W/L$ s.

Let  $X$  be the universe set of all sizes combinations of a VF and their performances. One can define a conventional set and three fuzzy sets on  $X$  as follows: Let  $P$  be a set of parameters defined by [31],

$$P = \{x \mid x = \{L(\mu m), I(\mu A), W(\mu m)\}\} \quad (1)$$

where  $I$  is the current bias ( $I_{ref}$  in Figure 1). Each  $x$  associates  $W/L$  sizes to perform an HSPICE™ simulation, which results are introduced into fuzzy sets as follows: The BWs are collected in  $\underline{A}$ , the fuzzy set of large BW, defined as

$$\underline{A} = \left\{ \frac{\mu_A(x)}{x} \mid x \text{ is a large bandwidth and } \mu_{\underline{A}}(x) = \frac{x}{\max BW} \right\}, \quad (2)$$

where  $\max BW$  is the maximum BW of all  $P$  sizes and the membership value of each BW,  $\mu_{\underline{A}}(x)$  depends on how much its value is large with respect to  $\max BW$ . The gains are collected in  $\underline{B}$ , the fuzzy set of gain close to unity, defined as

$$\underline{B} = \left\{ \frac{\mu_B(x)}{X} \mid x \text{ is a gain close to unity and } \mu_{\underline{B}}(x) = x \right\}, \quad (3)$$

where the membership value of each gain,  $\mu_{\underline{B}}(x)$  depends on how much its value is close to unity. The power consumptions are collected in  $\underline{C}$ , the fuzzy set of low PC, defined as

$$\underline{C} = \left\{ \frac{\mu_C(x)}{x} \mid x \text{ is a low power consumption and } \mu_{\underline{C}}(x) = \frac{\max PC - x}{\max Diff PC} \right\}, \quad (4)$$

where  $maxPC$  is the maximum PC of all  $P$  sizes, and  $maxDiffPC$  is the maximum difference between the  $maxPC$  and each PC of  $P$ , it means

$$maxPC = \max \{PC_1, PC_2, \dots, PC_P\} \text{ and} \quad (5)$$

$$maxDiffPC = \max \{maxPC - PC_1, maxPC - PC_2, \dots, maxPC - PC_P\} \quad (6)$$

Once calculated the fuzzy sets  $\tilde{A}$ ,  $\tilde{B}$  and  $\tilde{C}$ , in accordance with (2), (3) and (4), their intersection is defined as:

$$\tilde{T} = \tilde{A} \cap \tilde{B} \cap \tilde{C} = \left\{ \frac{\mu_T(x)}{x} \mid \mu_T(x) = \min \{ \mu_A(x), \mu_B(x), \mu_C(x) \} \right\} \quad (7)$$

The element from  $\tilde{T}$  with the maximum membership function represents the  $W/L$  sizes that best accomplish the three desired characteristics, i.e.:

$$OptWL = \max \{ \mu_T(x) \} \quad (8)$$

Before computing (2) - (8), the IC designer can select, from all  $P$  combinations, those values where the gain, BW and PC deviate from the maximum gain, the maximum BW and the minimum PC, respectively, in certain percentage (called  $des\_dis$ ). To do that we define three thresholds:

$$thr_{gain} = maxGain - \frac{des\_dis\_gain * \Delta_{gain}}{100} \quad (9)$$

$$thr_{BW} = maxBW - \frac{des\_dis\_BW * \Delta_{BW}}{100} \quad (10)$$

$$thr_{PC} = maxPC - \frac{des\_dis\_PC * \Delta_{PC}}{100} \quad (11)$$

where  $des\_dis\_gain$ ,  $des\_dis\_BW$ , and  $des\_dis\_PC$  are distances deviating desired percentages from the maximum gain, maximum BW and minimum PC, respectively.  $maxGain$  is the maximum gain;  $\Delta_{gain} = maxGain - minGain$ ,  $\Delta_{BW} = maxBW - minBW$ ,  $\Delta_{PC} = maxPC - minPC$ ;  $minGain$ ,  $minBW$  and  $minPC$  are the minimum gain, the minimum BW and the minimum PC, respectively. Thus, if for certain combination  $x_i \in P (i = 1, 2, \dots, |P|)$

$$gain_i \geq thr_{gain} \text{ and} \quad (12)$$

$$BW_i \geq thr_{BW} \text{ and} \quad (13)$$

$$PC_i \geq thr_{PC} \quad (14)$$

then these elements are stored in  $\tilde{A}$ ,  $\tilde{B}$  and  $\tilde{C}$ , otherwise they are not stored in the fuzzy sets and  $x_i$  is eliminated from  $P (P = P - \{x_i\})$ . The algorithm of our proposed approach is listed in Algorithm 1.

### 3. Experimental Results

Figure 1 shows three voltage followers, with the  $P$  set

$$P = \{L, I, \{W_A, W_B, W_C, W_D\}\} \quad (15)$$

where

$$\begin{aligned} L &= \{1.0\mu m\}, I = \{70\mu A\}, \\ W_A &= \{0.7\mu m, 7\mu m, 13.3\mu m, \dots, 107.8\mu m\}, \\ W_B &= \{0.7\mu m, 7\mu m, 13.3\mu m, \dots, 107.8\mu m\}, \\ W_C &= \{0.7\mu m, 7\mu m, 13.3\mu m, \dots, 107.8\mu m\}, \\ W_D &= \{0.7\mu m, 7\mu m, 13.3\mu m, \dots, 107.8\mu m\}. \end{aligned}$$

In generating the feasible solutions, one should verify that the  $W/L$  ratios of the P-MOSFETs are greater than or equal to the N-MOSFETs. It means:  $W_{M_1, M_2} \geq W_{M_3, M_4}$  for Figure 1(a),

$W_{M_1, M_4} \geq W_{M_2, M_3}$  for Figure 1(b), and  $W_{M_3, M_4} \geq W_{M_1, M_2}$  for Figure 1(c).

The results for Figure 1(a) and Figure 1(c) are shown in Figures 2 and 3, respectively. For Figure

1(b) we only list statistical values in the following. In all cases, the selected sizes are marked by considering several thresholds, and  $low\_bow = 0.9$ ; i.e. the selected sizes accomplishes “gain closer to unity”, “large bandwidth”, and “minimum power consumption” in the feasible solution space.

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#### Algorithm 1

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**Require:** values of  $L$ :  $L_1, L_2, \dots, L_P$   
 values of  $I$ :  $I_1, I_2, \dots, I_q$   
 values of  $W$ :  $W_1, W_2, \dots, W_r$   
**Ensure:** optimum value of  $L, I, W$ :  $optL, optI, optW$   
 optimum value of gain( $A_v$ ), BW and PC:  $optGa, optBW, optPC$

1. BEGIN  
 /\*Define all W/L combinations in  $P^*$ \*/
2.  $P \leftarrow \left\{ (L_i, I_j, W_k) \mid i = 1, 2, \dots, p; j = 1, 2, \dots, q; k = 1, 2, \dots, r \right\}$   
 /\* Select  $A_v$ , BW and PC from HSPICE™ simulations for each  $P$  combination \*/
3. **for**  $i = 1 \rightarrow |P|$  **do**
4.    $[A_{v\_set}(i), BW\_set(i), PC\_set(i)] \leftarrow HSPICE(P(i))$
5. **end for**
6.   /\* Compute Thresholds according to (12), (13) and (14) \*/
7.    $[minGain, maxGain] \leftarrow minMax(A_{v\_set})$
8.    $[minBW, maxBW] \leftarrow minMax(BW\_set)$
9.    $[minPC, maxPC] \leftarrow minMax(PC\_set)$
10.   Compute  $thr_{gain}, thr_{BW}, thr_{PC}$  according to (12), (13) and (14)
11.   /\* Delete combinations which do not meet with (12), (13) and (14) \*/
12.   **for**  $i = 1 \rightarrow |P|$  **do**
13.    **if**  $\neg (A_{v\_set}(i) \geq thr_{gain} \text{ and } BW\_set(i) \geq thr_{BW} \text{ and } PC\_set(i) \geq thr_{PC})$  **then**
14.       $A_{v\_set} \leftarrow A_{v\_set} - \{A_{v\_set}(i)\}$
15.       $BW\_set \leftarrow BW\_set - \{BW\_set(i)\}$
16.       $PC\_set \leftarrow PC\_set - \{PC\_set(i)\}$
17.    **end if**
18.   **end for**
19.   /\*Compute fuzzy sets according to (2), (3), (4)\*/
20.    $maxDiffPC \leftarrow \max \{maxPC - PC_1, maxPC - PC_2, \dots, maxPC - PC_p\}$
21.    $Bfuzzy \leftarrow A_{v\_set}$
22.   **for**  $i = 1 \rightarrow |P|$  **do**
23.     $Afuzzy(i) \leftarrow BW\_set(i) / maxBW$
24.     $Cfuzzy(i) \leftarrow (maxPC - PC\_set(i)) / maxDiffPC$
25.   **end for**
26.   /\*Compute the intersection of fuzzy sets\*/

```

23. for  $i = 1 \rightarrow |P|$  do
24.      $T(i) = \min \{A_{fuzzy}(i), B_{fuzzy}(i), C_{fuzzy}(i)\}$ 
25. end for

/*Compute the optimum  $W/L$  sizes*/
26.  $[opt, index] \leftarrow \max \{T\}$ 
27.  $[optL, optI, optW] \leftarrow [opt(index).Lvalue, opt(index).Ivalue, opt(index).Wvalue]$ 
28.  $[optGa, optBW, optPC] \leftarrow [A_v\_set(index), BW\_set(index), PC\_set(index)]$ 
29. END
    
```

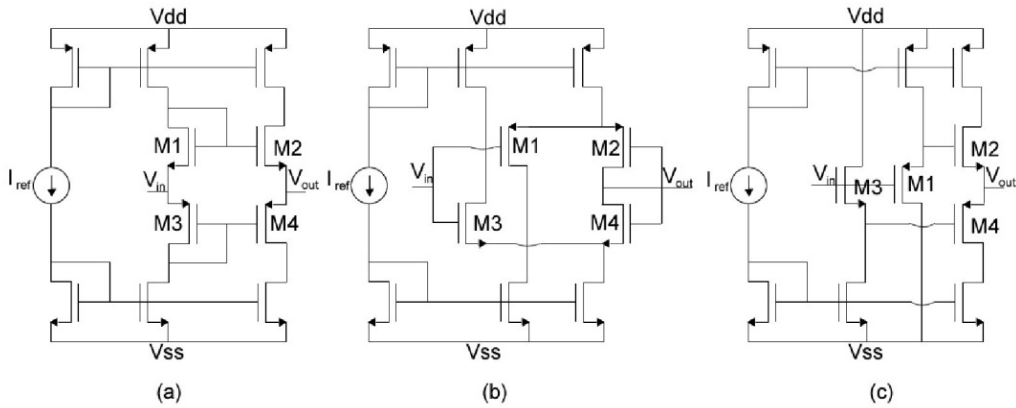


Figure 1. Voltage followers taken from [12].

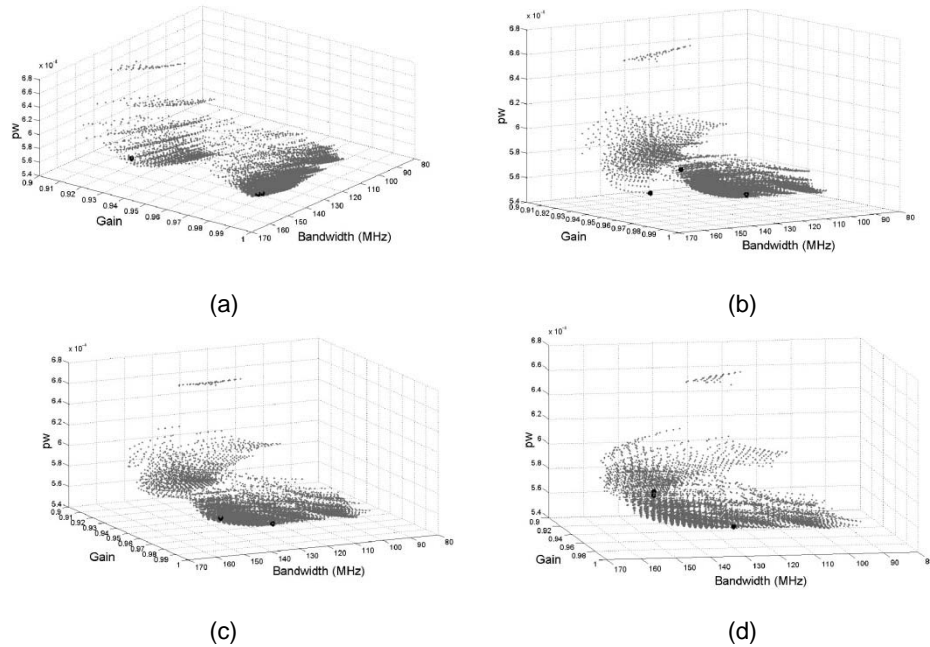


Figure 2. Voltage followers taken from [12].

Statistical details are provided in Tables 1-3, with  $L = 1\mu\text{m}$  and  $I = 70\mu\text{A}$ . For instance, good results are shown in Figure 2(a), where  $des\_dis = 1\%$  for the gain ( $A_v$ ),  $des\_dis = 1\%$  for BW and  $1\%$  for PC ( $A_v=0.9921$ ,  $BW=154.9\text{MHz}$ ,  $PC = 572.09\mu\text{W}$ ), this can be observed clearly in Table 1. Our proposed method selected the individual that is slightly far from the maximum gain, maximum BW and minimum PC. Another good result is when  $des\_dis = 10\%$  for the gain,  $des\_dis = 10\%$  for BW and  $des\_dis = 10\%$  for PC ( $A_v= 0.9917$ ,  $BW=156.7\text{MHz}$ ,  $PC = 573.1\mu\text{W}$ ). In this case the selected individual improves the BW, but the gain is reduced and the PC augmented. However, when  $des\_dis$  is not used, the result is  $A_v = 0.9232$ ,  $BW=146.2\text{MHz}$ , and  $PC=555.38\mu\text{W}$ .

To select the best solution accomplishing one objective, one can provide different percentages (thresholds). For example, in Figure 2(b) at which each solution is reflected in Table 1, giving  $des\_dis = 1\%$  for the gain,  $des\_dis = 99\%$  for BW

and  $des\_dis = 99\%$  for PC, the selected individual has  $A_v=0.993$ ,  $BW=138\text{MHz}$  and  $PC=562.79\mu\text{W}$ , this shows the best individual accomplishing “gain closer to unity”. To select an individual accomplishing the highest BW, one can provide  $des\_dis = 99\%$  for the gain,  $des\_dis = 1\%$  for BW and  $des\_dis = 99\%$  for PC, leading to  $A_v=0.9889$ ,  $BW=162.2\text{MHz}$ , and  $PC=587.13\mu\text{W}$ , so that this individual accomplishes “maximum bandwidth”. To select “minimum power consumption” one can provide  $des\_dis = 99\%$  for the gain,  $des\_dis = 99\%$  for BW and  $des\_dis = 1\%$  for PC ( $A_v=0.9101$ ,  $BW=125.9\text{MHz}$ ,  $PC=541.51\mu\text{W}$ ).

From Table 2, a good result is when  $des\_dis = 1\%$  for the gain,  $des\_dis = 1\%$  for BW and  $des\_dis = 1\%$  for PC ( $A_v=0.9859$ ,  $BW=53.09\text{MHz}$ ,  $PC=462.52\mu\text{W}$ ).

As one can infer, by using low distances or percentages for the objectives, the proposed method selects individuals accomplishing “close to

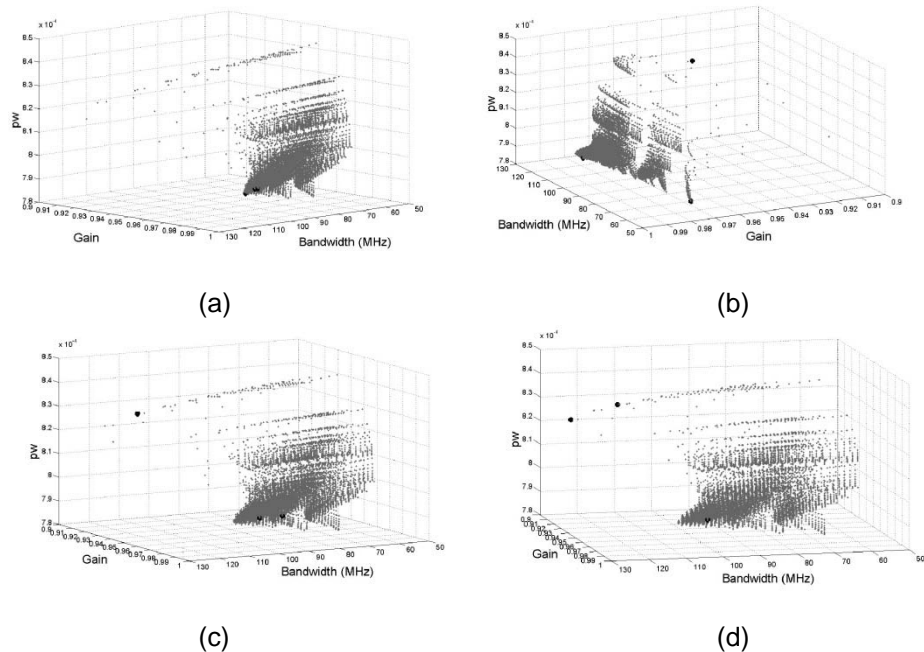


Figure 3. Selected feasible sizes solutions for the VF in Figure 1(c).

unity", "maximum bandwidth" and "minimum power consumption". However, by increasing the distance or percentage, the performance of the selected individual is reduced.

Table 3 shows results for Figure 1(c). With  $des\_dis = 0\%$ , the results are  $A_v = 0.9861$ ,  $BW = 108.4\text{MHz}$  and  $PC = 791.17\mu\text{W}$ . Otherwise, if  $des\_dis = 1\%$  for the gain,  $des\_dis = 1\%$  for BW and  $des\_dis = 1\%$  for PC, the selected individual

performs  $A_v = 0.9899$ ,  $BW = 107.2\text{MHz}$ , and  $PC = 793.58\mu\text{W}$ .

### 3.1 Current Feedback Operational Amplifier (CFOA)

To show the behavior of the proposed method with an evolved circuit, we present the selection of the optimal  $W/L$  sizes of a CFOA. As already shown in [14], a CFOA is designed from the cascade connections of VF + CM + VF, where CM denotes a current mirror.

Solutions	BW MHz	$A_v$	PC $\mu\text{W}$	$W_{3,4}$ $\mu\text{m}$	$W_{1,2}$ $\mu\text{m}$	Des_dis $A_v$ -BW-PC
Figure 2(a)	146.2	0.9232	555.38	28.7	28.7	without
	154.9	0.9921	572.09	77.7	77.7	1%-1%-1%
	156.7	0.9917	573.1	77.7	63.7	10%-10%-10%
Figure 2(b)	138	0.993	562.79	98.7	98.7	1%-99%-99%
	162.2	0.9889	587.13	63.7	63.7	99%-1%-99%
	125.9	0.9101	541.51	21.7	21.7	99%-99%-1%
Figure 2(c)	154.9	0.9921	572.09	77.7	77.7	50%-10%-10%
	136.5	0.993	562.19	98.7	98.7	50%-50%-10%
	136.5	0.993	562.19	98.7	98.7	99%-50%-50%
Figure 2(d)	131.8	0.9912	561.01	98.7	35.7	10%-99%-10%
	154.9	0.9912	591.63	98.7	84.7	50%-10%-99%
	154.9	0.9912	588.5	98.7	77.7	99%-10%-50%

Table 1. Feasible sizes for Figure 1(a).

Solutions	BW MHz	$A_v$	PC $\mu\text{W}$	$W_{3,4}$ $\mu\text{m}$	$W_{1,2}$ $\mu\text{m}$	Des_dis $A_v$ -BW-PC
Case 1	48.98	0.9846	451.55	36.05	36.05	without
	53.09	0.9859	462.52	61.25	61.25	1%-1%-1%
	50.12	0.9882	455.81	99.05	99.05	10%-10%-10%
Case 2	49.55	0.9883	450.38	99.05	99.05	1%-99%-99%
	53.7	0.9837	490.28	61.25	61.25	99%-1%-99%
	22.39	0.9427	445.61	4.55	4.55	99%-99%-1%
Case 3	50.12	0.9882	455.81	99.05	99.05	50%-10%-10%
	49.55	0.9883	453.08	99.05	99.05	50%-50%-10%
	49.55	0.9883	453.08	99.05	99.05	99%-50%-50%
Case 4	49.55	0.9883	450.38	99.05	99.05	10%-99%-10%
	50.12	0.9851	478.67	99.05	99.05	50%-10%-99%
	50.12	0.9875	467.26	99.05	99.05	99%-10%-50%

Table 2. Feasible sizes for Figure 1(b).



Solutions	BW MHz	$A_v$	PC $\mu W$	$W_{3,4}$ $\mu m$	$W_{1,2}$ $\mu m$	Des_dis $A_v$ -BW-PC
Figure 3(a)	108.4	0.9861	791.17	36.05	36.05	Without
	107.2	0.9899	793.58	80.15	54.95	1%-1%-1%
	105.9	0.9897	793.39	73.85	67.55	10%-10%-10%
Figure 3(b)	102.3	0.9903	793.74	86.45	86.45	1%-99%-99%
	127.4	0.9291	825.83	23.45	23.45	99%-1%-99%
	66.83	0.9691	781.56	10.85	4.55	99%-99%-1%
Figure 3(c)	124.5	0.9475	833.29	29.75	23.45	50%-10%-10%
	93.33	0.9872	793.14	86.45	10.85	50%-50%-10%
	102.3	0.9903	793.74	86.45	86.45	99%-50%-50%
Figure 3(d)	102.3	0.9903	793.74	86.45	86.45	10%-99%-10%
	120.2	0.9576	837.53	36.05	29.75	50%-10%-99%
	127.4	0.9291	825.83	23.45	23.45	99%-10%-50%

Table 3. Feasible sizes for Figure 1(c).

The CFOA depicted in Figure 4 includes two VFs: one between nodes Y and X, and a second one between nodes Z and W, while a current mirror is placed between nodes X and Z. The encoding of the W/L sizes is shown in Table 4 [24]. This CFOA was designed using standard CMOS technology of 180nm,  $V_{ss} = -V_{dd} = 2$ ,  $I_{ref} = 50 \mu A$  and load capacitor of  $1 pF$ . The results of the selection of feasible sizes, using the proposed method, are shown in Figure 5. Statistical results are provided in Table 5 that corresponds to the VFs between nodes Y to X, and between nodes Z to W.

Table 5 shows the results by using different values for  $des\_dis$  in  $A_v$ , so that one could select the result with 10% in  $A_v$ , where  $A_v = 0.9877$  and  $BW = 734 MHz$ , for the VF between nodes X and Y. For the VF between nodes Z and W, one could select the result with  $des\_dis$  in  $A_v = 5\%$ , where  $A_v = 0.9871$  and  $BW = 783 MHz$ . In both cases for selecting the result with the best  $A_v$ , one could use  $des\_dis$  with 2%, otherwise, if one needs the best Bandwidth, one could use the method without the percentage for  $des\_dis$ , i.e.  $des\_dis = 0\%$ .

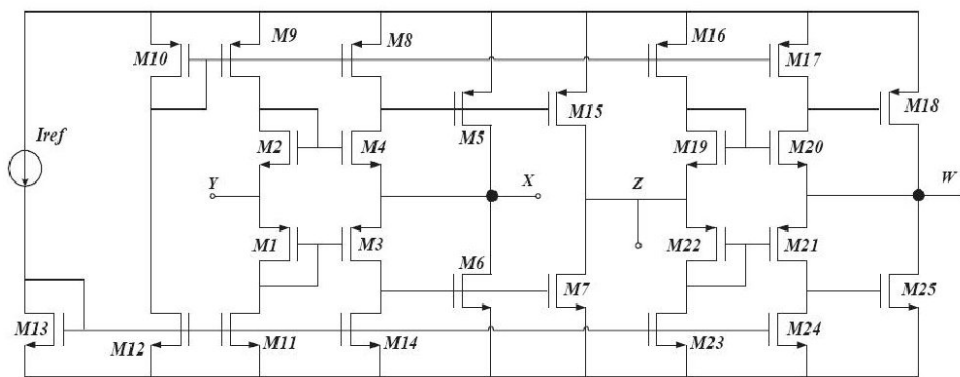
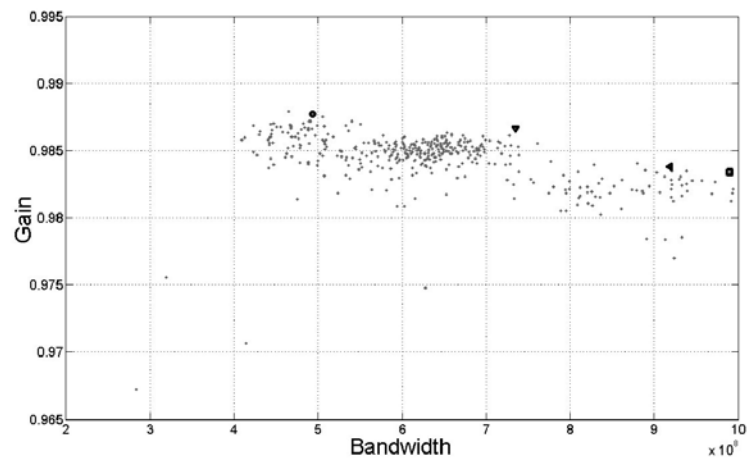


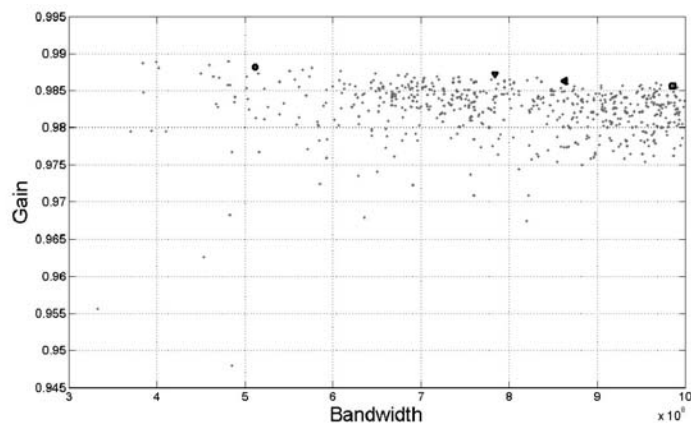
Figure 4. Current-Feedback Operational Amplifier (CFOA).

gene	Design Variable	Encoding Transistors
$x_1$	L	$M_1, \dots, M_{25}$
$x_2$	$W_1$	$M_{11}, M_{12}, M_{13}, M_{14}$
$x_3$	$W_2$	$M_8, M_9, M_{10}$
$x_4$	$W_3$	$M_6$
$x_5$	$W_4$	$M_5$
$x_6$	$W_5$	$M_1, M_3$
$x_7$	$W_6$	$M_2, M_4$
$x_8$	$W_7$	$M_{15}$
$x_9$	$W_8$	$M_7$
$x_{10}$	$W_9$	$M_{23}, M_{24}$
$x_{11}$	$W_{10}$	$M_{16}, M_{17}$
$x_{12}$	$W_{11}$	$M_{21}, M_{22}$
$x_{13}$	$W_{12}$	$M_{19}, M_{20}$
$x_{14}$	$W_{13}$	$M_{18}$
$x_{15}$	$W_{14}$	$M_{25}$

Table 4. Feasible sizes for Figure 1(c)



(a)



(b)

Figure 5. Selected feasible sizes solutions for the CFOA from Figure 4.

<i>Des_dis</i> Parameters	VF <sub>YX</sub>				VF <sub>ZW</sub>			
	without	2%	10%	20%	without	2%	5%	7%
BW	9.89E+8	4.93E+8	7.34E+8	9.18E+8	9.85E+8	5.11E+8	7.83E+8	8.63E+8
A <sub>v</sub>	.9833	.9877	.9866	.9838	.9856	.9881	.9871	.9862
Variable Values								
L	3.60E-7	7.20E-7	5.40E-7	3.60E-7	5.40E-7	7.20E-7	5.40E-7	5.40E-7
W <sub>1</sub>	4.82E-6	3.11E-6	2.71E-6	4.37E-6	8.02E-6	1.15E-5	4.13E-6	7.10E-6
W <sub>2</sub>	7.38E-5	7.11E-5	7.41E-5	6.57E-5	6.66E-5	7.53E-5	6.41E-5	7.14E-5
W <sub>3</sub>	3.13E-5	3.91E-5	5.79E-5	3.77E-5	4.03E-5	6.75E-5	3.23E-5	3.50E-5
W <sub>4</sub>	4.41E-5	4.23E-5	6.09E-5	3.94E-5	8.15E-6	1.65E-5	2.29E-5	2.47E-5
W <sub>5</sub>	7.57E-5	7.49E-5	7.15E-5	6.20E-5	7.52E-5	4.56E-5	6.33E-5	5.54E-5
W <sub>6</sub>	1.33E-5	1.93E-5	1.81E-5	2.43E-5	4.26E-5	2.81E-5	2.95E-5	5.78E-6
W <sub>7</sub>	2.80E-5	3.73E-5	3.29E-5	3.97E-5	2.83E-5	6.00E-5	7.98E-5	2.51E-5
W <sub>8</sub>	3.94E-5	4.16E-5	3.53E-5	4.30E-5	5.14E-6	1.51E-5	5.38E-5	1.79E-5
W <sub>9</sub>	7.56E-6	4.92E-6	4.96E-6	1.49E-5	8.89E-6	1.53E-5	1.94E-6	8.50E-6
W <sub>10</sub>	6.22E-5	6.09E-5	7.52E-5	6.41E-5	7.85E-5	6.54E-5	6.66E-5	6.00E-5
W <sub>11</sub>	5.64E-5	2.56E-5	1.74E-5	3.27E-5	6.01E-5	6.57E-5	7.93E-5	5.30E-5
W <sub>12</sub>	2.95E-5	5.09E-5	7.90E-5	4.85E-5	5.92E-5	6.67E-5	2.10E-5	5.83E-5
W <sub>13</sub>	2.31E-5	4.02E-5	4.80E-5	6.22E-5	6.67E-5	4.39E-5	2.75E-5	5.12E-5
W <sub>14</sub>	5.63E-5	6.20E-5	5.80E-5	4.34E-5	5.13E-5	4.09E-6	1.33E-5	1.14E-5

Table 5. Feasible sizes of the CFOA from Figure 4.

#### 4. Conclusions

An automatic method focused on the intersection among (three) fuzzy sets has been introduced to solve for the open problem of selecting feasible W/L MOSFET sizes for analog ICs. For the case of voltage followers, we highlighted their representation under several ranges of values of W/L, and current bias using three fuzzy sets to represent: large bandwidth, gain closer to unity and minimum power consumption. As a result, by performing our proposed fuzzy sets intersection approach, we showed how to select feasible solutions to accomplish the gain closer to unity, maximum bandwidth and minimum power consumption. It was demonstrated that the main advantage is devoted to the interacting process

where the analog IC designer provides desired distances *des\_dis* from the required objective, then the intersection procedure selects individuals allowing moving among the feasible sizes solutions space. The proposed sizes-selection approach was extended to a big circuit named current-feedback operational amplifier, for which the selected W/L sizes accomplishes desired target specifications. Finally, we can conclude that the selected sizes can enhance the performances of the active devices in realizing linear and nonlinear circuit applications.

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## References

- [1] Tlelo-Cuautle E. *Analog Integrated Circuits for Analog Signal Processing*, Springer, June 2012.
- [2] Tlelo-Cuautle E. *Advances in Analog Circuits*, InTech Publisher, February 2011. Open Access <http://www.intechweb.org/books/show/title/advances-in-analog-circuits>
- [3] Sánchez-López C, Fernández F.V, Tlelo-Cuautle E, Tan S XD, Pathological Element-Based Active Device Models and Their Application to Symbolic Analysis, *IEEE Trans on Circuits and Systems I: Regular papers*, vol. 58, no. 6, pp. 1382-1395, June 2011.
- [4] Sánchez-López C, Tlelo-Cuautle E, Martínez-Romero E. Symbolic Analysis of OTRAs-Based Circuits, *Journal of Applied Research and Technology*, vol. 9, no. 1, pp. 69-80, April 2011.
- [5] Pathak J.K, Singh A.K, Senani R. Systematic realisation of quadrature oscillators using current differencing buffered amplifiers, *IET Circuits, Devices and Systems*, vol. 5, no. 3, pp. 203-211, 2011.
- [6] Swamy M.N.S. Mutators, Generalized Impedance Converters and Inverters, and Their Realization Using Generalized Current Conveyors, *Circuits, Systems, and Signal Processing*, vol. 30, no. 1, pp. 209-232, 2011.
- [7] Khateb F, Bielek D. Bulk-Driven Current Differencing Transconductance Amplifier, *Circuits, Systems, and Signal Processing*, vol. 30, no. 5, pp. 1071-1089, 2011.
- [8] Becerra-Alvarez E, Sandoval-Ibarra F, de la Rosa Jose M. Design of an adaptive LNA for hand-held devices in a 1-V 90-nm standard RF CMOS technology: From circuit analysis to layout, *Journal of Applied Research and Technology*, vol. 7, no. 1, pp. 51-61, April 2009.
- [9] Mateos-Santillan E, Perez-Silva J.L. Design, at transistor level, of a neuron with axonic delay, *Journal of Applied Research and Technology*, vol. 7, no. 1, pp. 62-72, April 2009.
- [10] Campos-Canton I. Development of logical cells through state space in a two-dimensional system, *Revista Mexicana de Fisica*, vol. 57, no. 2, pp. 106-109, April 2011.
- [11] Ghafar-Zadeh E, Sawan M, Therriault D. CMOS based capacitive sensor laboratory-on-chip: a multidisciplinary approach, *Analog Integrated Circuits and Signal Processing*, vol. 59, no. 1, pp. 1-12, 2009.
- [12] Tlelo-Cuautle E, Duarte-Villaseñor M.A, Guerra-Gómez I. Automatic synthesis of VFs and VMs by applying genetic algorithms, *Circuits, Systems, and Signal Processing*, vol. 27, no. 3, pp. 391--403, June 2008.
- [13] Tlelo-Cuautle E, Moro-Frias D, Sánchez-López C, Duarte-Villaseñor M.A. Synthesis of CCII-s by superimposing VFs and CFs through genetic operations, *IEICE Electron. Express*, vol. 5, no. 11, pp. 411-417, June 2008.
- [14] Duarte-Villaseñor M.A, Tlelo-Cuautle E, de la Fraga L.G. Binary genetic encoding for the synthesis of mixed-mode circuit topologies, *Circuits, Systems, and Signal Processing*, vol. 31, no. 3, pp. 849-863, 2012.
- [15] Tlelo-Cuautle, E., Duarte-Villaseñor, M.A.: Evolutionary electronics: automatic synthesis of analog circuits by GAs. In: Yang Ang, B.L.T., Yin, S. (eds.) Success in Evolutionary Computation. SCI, pp. 165–188. IGI Global (2008)
- [16] Sánchez-López C, Castro-Hernández A, Pérez-Trejo A. Experimental verification of the chua's circuit designed with UGCs, *IEICE Electron. Express*, vol. 5, no. 17, pp. 657--661, 2008.
- [17] Trejo-Guerra R, Tlelo-Cuautle E, Cruz-Hernández C, Sanchez-López C. Chaotic communication system using chua's oscillators realized with CCII+s, *International Journal of Bifurcations and Chaos*, vol. 19, no. 12, pp. 4217-4226, December 2009.
- [18] Trejo-Guerra R, Tlelo-Cuautle E, Jiménez-Fuentes J.M, Muñoz-Pacheco J.M, Sánchez-López C. Multiscroll Floating Gate Based Integrated Chaotic Oscillator, *International Journal of Circuit Theory and Applications*, 2011. DOI: 10.1002/cta.821
- [19] Gonzalez-Ramirez R.G, Smith N.R, Askin R.G, Miranda P.A, Sánchez J.M. A Hybrid Metaheuristic Approach to Optimize the Districting Design of a Parcel Company, *Journal of Applied Research and Technology*, vol. 9, no. 1, pp. 19-35, April 2011.
- [20] Laguna-Sanchez G.A, Olguin-Carbajal M, Cruz-Cortes N, Barrón-Fernández R, Alvarez-Zedillo J.A. Comparative Study of Parallel Variants for a Particle Swarm Optimization Algorithm Implemented on a Multithreading GPU, *Journal of Applied Research and Technology*, vol. 7, no. 3, pp. 292-309, December 2009.
- [21] Fakhfakh M, Cooren Y, Sallem A, Loulou M, Siarry P. Analog circuit design optimization through the particle swarm optimization technique, *Analog Integrated Circuits and Signal Processing*, vol. 63, no. 1, pp. 71-82, 2010.

- [22] Tlelo-Cuautle E, Guerra-Gómez I, Reyes-García C.A, Duarte-Villaseñor M.A. Synthesis of Analog Circuit by Genetic Algorithms and their Optimization by Particle swarm Optimization, in *Intelligent System for Automated Learning and Adaptation: Emerging Trends and Applications*, Chiong R (Ed.), pp. 173-192, IGI Global, 2010. DOI: 10.4018/978-1-60566-798-0.ch008
- [23] Tlelo-Cuautle E, Guerra-Gómez I, Duarte-Villaseñor M.A, de la Fraga L.G, Flores-Becerra G, Reyes-Salgado G, Reyes-García C.A, Rodríguez-Gómez G. Applications of evolutionary algorithms in the design automation of analog integrated circuits, *Journal of Applied Sciences*, vol. 10, no. 17, pp. 1859-1872, 2010.
- [24] Tlelo-Cuautle E, Guerra-Gómez I, de la Fraga L.G, Flores-Becerra G, Polanco-Martagón S, Fakhfakh M, Reyes-García C.A, Rodríguez-Gómez G, Reyes-Salgado G. Evolutionary Algorithms in the Optimal Sizing of Analog Circuits, in *Intelligent Computational Optimization in Engineering*, Koeppen M, Schaefer G, Abraham A (Eds.), vol. 366, pp. 109-138, Springer, 2011. DOI: 10.1007/978-3-642-21705-0\_5
- [25] Sonmez-Ozsun S, Dundar Gunhan. Simulation-based analog and RF circuit synthesis using a modified evolutionary strategies algorithm, *Integration-The VLSI Journal*, vol. 44, no. 2, pp. 144-154, March 2011.
- [26] Liu B, Fernández F.V, Gielen G.E. Efficient and Accurate Statistical Analog Yield Optimization and Variation-Aware Circuit Sizing Based on Computational Intelligence Techniques, *IEEE Trans on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 6, pp. 793-805, June 2011.
- [27] Rangel D, Rivera A.L, Alaniz P.D. Intelligent Positioning Fuzzy Servomechanism Under PWM Nonlinear Loads, *Journal of Applied Research and Technology*, vol. 8, no. 1, pp. 87-100, 2010.
- [28] Perez S.J.L, Garces M.A, Cabiedes C.F, Miranda A.V. Electronic model of a dubois fuzzy integration neuron, *Journal of Applied Research and Technology*, vol. 7, no. 1, pp. 73-82, April 2009.
- [29] Torralba A, Chavez J, Franquelo L. Fasy: a fuzzy logic based tool for analog synthesis, *IEEE Trans on Computer-Aided Design of Integrated Circuits and Systems*, vol. 15, no. 7, pp. 705-715, 1996.
- [30] Diaz-Madrid J.A, Hinojosa J, Doménech-Asensi G. Fuzzy logic technique for accurate analog circuits macromodel sizing, *International Journal of Circuit Theory and Applications*, vol. 38, no. 3, pp. 307-319, April 2010.
- [31] Polanco-Martagón S, Flores-Becerra G, Tlelo-Cuautle E. Fuzzy-Set Based Approach to Compute Optimum Sizes of Voltage Followers, in *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 844-847, Tunisia 2009.