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Active pre-filters for dc/dc Boost regulators

Pre-filtros activos para reguladores dc/dc elevadores

C. A. Ramos-Paja[1], R. Giral[2] and C. Carrejo[3]

ABSTRACT

This paper proposes an active pre-filter to mitigate the current harmonics generated by classical dc/dc Boost regulators, which generate current ripples proportional to the duty cycle. Therefore, high output voltage conditions, i.e., high voltage conversion ratios, produce high current harmonics that must be filtered to avoid damage or source losses. Traditionally, these current components are filtered using electrolytic capacitors, which introduce reliability problems because of their high failure rate. The solution introduced in this paper instead uses a dc/dc converter based on the parallel connection of the Boost canonical cells to filter the current ripples generated by the Boost regulator, improving the system reliability. This solution provides the additional benefits of improving the overall efficiency and the voltage conversion ratio. Finally, the solution is validated with simulations and experimental results.

Keywords: Boost regulator, parallel connection, active pre-filter, dc/dc power converter.

RESUMEN

Este artículo propone un pre-filtro activo para mitigar los armónicos de corriente generados por reguladores elevadores clásicos, los cuales producen rizados de corriente proporcionales al ciclo de trabajo. Por tanto, altos voltajes de salida, i.e., altos factores de transformación de voltaje, producen armónicos de corriente que se deben filtrar para evitar daños o pérdidas de potencia en la fuente. Tradicionalmente, estas componentes se filtran usando condensadores electrolíticos, lo que introducen problemas de confiabilidad debido a su alta taza de falla. En contraste, la solución propuesta usa un convertidor dc/dc, basado en la conexión paralela de celdas canónicas Boost, para filtrar el rizado de corriente generado por el regulador Boost, lo que mejora la confiabilidad del sistema. Esta solución, además, incrementa la eficiencia total y el factor de transformación de voltaje. Finalmente, la solución se valida usando simulaciones y resultados experimentales.

Palabras clave: Regulador Boost, conexión paralela, pre-filtro activo, convertidor de potencia dc/dc.

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Introduction

DC loads, such as those in electronics equipment, require regulated dc power to operate correctly, but it is difficult to find dc sources that provide regulated voltage and/or current. Therefore, a large number of dc power regulators have been proposed in the literature (Veerachary et al., 2003), (Taghvaee et al., 2013). Among them, the Boost regulator is the most widely adopted regulator that supplies dc loads requiring voltages higher than the source voltage. The extensive use of the Boost regulator is due to its simple circuitry and simple control, but it exhibits three main drawbacks (Veerachary et al., 2003): its voltage conversion ratio is strongly restricted for relatively small parasitic losses, its operation at high voltages requires duty cycles near saturation, and it produces high current harmonics at the source.

These current harmonics introduce problems for classical sources such as batteries by degrading the source lifetime and generating a sensible problem in portable applications (Kuperman and Aharon, 2011). Similarly, the growth of renewable energy sources has forced the design of high-boosting/low-ripple dc/dc regulators: photovoltaic panels and fuel cells provide low-voltage/high-current dc power, which must be transformed to high-voltage levels to be injected into the grid. In addition, fuel cells are damaged by high current harmonics (Ramos-Paja et al., 2009), while the power generated by photovoltaic panels is strongly reduced in presence of current ripples (Aranda et al., 2009).

Consider the classical Boost regulator in Figure 1. Its input current ripple H_{CR} is given by (1), where D_{CR} is the duty cycle and R_L models the parasitic losses. From (1), it is noted that high output voltages (high D_{CR}) produce high current ripples.

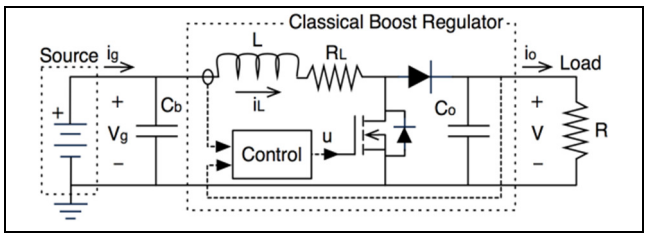

Figure 1. Classical Boost Regulator

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This problem has been addressed in two ways: first, using large capacitors to filter the current harmonics (C_b in Figure 1) requires electrolytic technology that introduces reliability problems because its high failure rate (Petrone et al. 2008). Second, designing the complex dc/dc converters (Arango et al. 2012) greatly increases the complexity of the circuit analysis and regulation control.

$$H_{CR} = \frac{V_g \cdot D_{CR}}{L} \cdot \left(1 - \frac{R_L / R}{(1 - D_{CR})^2 + (R_L / R)} \right) \qquad (1)$$

This paper proposes a balanced solution to introduce a self-controlled active pre-filter without affecting the regulator's complexity and control. The solution is based on the parallel connection of the canonical Boost cells, which are controlled with a programmed current control. In addition to its filtering capability, the proposed pre-filter improves the overall efficiency and allows the regulator to provide higher output voltages. Moreover, because electrolytic capacitors are not required, the system reliability is not affected.

Active pre-filter based on parallel converters

The proposed pre-filter is based on the parallel connection of multiple Boost converters. This topology was selected because of its continuous input current and triangular waveform. Then, the converters must be operated to mitigate the current ripple of one converter with the current ripple generated by the other converters, which eventually generates a ripple-free input current. Thus, any power source connected at the pre-filter input will be protected from the current harmonics generated by any load connected at the pre-filter output.

Figure 2 shows the pre-filter structure. The canonical cell is formed by a Boost topology in which the inductor's equivalent series resistance (ESR) collects all the converter losses. This canonical cell is used to construct an N-order filter, where N is the number of cells in parallel. Hence, all the cells have the same input and output voltages and eventually the same duty cycle.

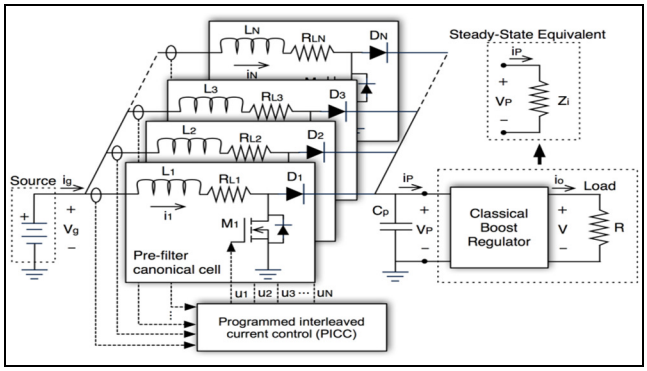

Figure 2. Pre-filter structure

Therefore, the cells' input current (i.e., inductor currents) must be shifted to match the high part of some cells' ripples with the low part of the other cells' ripples. Thus, the cells' ripples are cancelled to produce a ripple-free input current.

In addition, the average currents of all the cells must be the same to avoid overcharging one (or several) cell(s), which could lead to a destructive condition: if a cell is overcharged, its inductor and/or switches (MOSFET and diode) could be damaged; hence, the remaining cells will support an increased current, which could damage more cells. To prevent this destructive condition, the pre-filter is regulated to ensure the same average current in all the cells. Figure 2 shows the connection of the programed interleaved current control (PICC) proposed to regulate the pre-filter, which ensures the same current on all the cells. This controller is explained in detail below.

Finally, the pre-filter load could be modeled with a differential resistance Zi that represents the input impedance of the main Boost regulator. In the following sections, the expressions that describe the inductor currents are obtained and used to calculate the optimal shift time for the parallel cells.

Single-cell analysis

For the system shown in Figure 2, the cell inductor current i_1 is given by (2), where I_1 represents the average cell current, H represents the amplitude of the current ripple given in (3), D represents the duty cycle, and T represents the switching period.

$$i_1 = \begin{cases} \frac{1}{L_1}\left(V_g - I_1 \cdot R_{L1}\right) \cdot t - \frac{H}{2} + I_1, 0 \le t \le D \cdot T \\ \frac{1}{L_1}\left(V_g - I_1 \cdot R_{L1} - V_P\right) \cdot t + \frac{H}{2} + I_1, D \cdot T \le t \le T \end{cases} \qquad (2)$$

$$H = \frac{1}{L_1}\left(V_g - I_1 \cdot R_{L1}\right) \cdot D \cdot T \qquad (3)$$

In addition, the pre-filter output current i_P is uniformly divided among all the cells. Therefore, the average current in diode D_1 is given by $I_{D1} = (V_P/Zi)/N$, which leads to the average inductor current given in (4).

$$I_1 = \left(V_P / Zi\right) / \left(N \cdot D\right) \qquad (4)$$

Then, using the charge and volt-second balances (Erickson and Maksimovic, 2001), the cell voltage conversion ratio $M(D)_C$ is given by (5).

$$M(D)_C = \frac{1}{1 - D + \frac{\left(R_{L1} / Zi\right)}{D \cdot N}} \qquad (5)$$

Shift time and duty cycle for N = 2

To illustrate the calculation of the shift time and duty cycle required to cancel out the inductor current ripples, the second-order pre-filter (N = 2) is used. Thus, the second cell current i_2 is shifted in ΔT seconds, obtaining the expression given in (6), where the average values of both i_1 and i_2 are the same.

$$i_2 = \begin{cases} \frac{1}{L_1}\left(V_g - I_1 \cdot R_{L1}\right) \cdot \left(t - \Delta T\right) - \frac{H}{2} + I_1, 0 \le t \le D \cdot T \\ \frac{1}{L_1}\left(V_g - I_1 \cdot R_{L1} - V_P\right) \cdot \left(t - \Delta T\right) + \frac{H}{2} + I_1, D \cdot T \le t \le T \end{cases} \qquad (6)$$

Figure 3(a) illustrates the effect of ΔT on the input current i_g: because the shift time is not optimal, the high and low peaks of both i_1 and i_2 are not compensated, generating an input current ripple equal to H. In addition, if $\Delta T = 0$ s, both i_1 and i_2 are in phase, producing a ripple in i_g equal to 2H.

By considering that $i_g = i_1 + i_2$, the mitigation of the current ripple in i_g is obtained for $i_1 + i_2 = 2I_1 = 2I_2$. Then, replacing (2) and (6) in $i_1 + i_2 - 2I_1 = 0$ leads to $\Delta T = DT$. This condition indicates that the high peak of i_1 must coincide with the low peak of i_2 (and vice-versa) to ensure the ripple's cancelation. Moreover, because there are two cells, each period must exhibit two ΔT time shifts: a first shift

ΔT between i_1 and i_2 and a second shift ΔT between i_2 and i_1, which leads to:

$$T=2\cdot\Delta T=2\cdot D\cdot T\Rightarrow D=1/2 \quad (7)$$

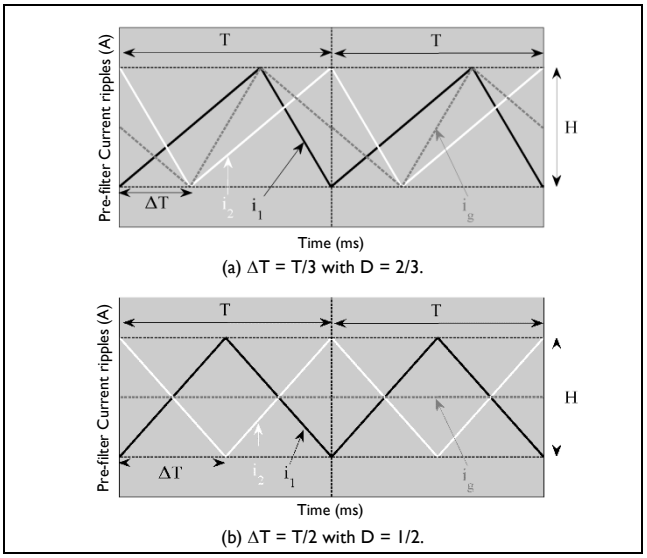

Figure 3. Behavior of the second-order pre-filter (N = 2)

From (7), it is concluded that the cells must be operated with a duty cycle D = 1/2 with a shift time $\Delta T = T/2$. Figure 3(b) shows this condition, where the input current i_g does not exhibit any ripples because of the cancelation between the i_1 and i_2 ripples.

Shift time and duty cycle for N ≥ 3

The second-order pre-filter has a single optimal operating condition (ΔT, D), but the high-order (N ≥ 3) pre-filters exhibit more than one optimum. This characteristic is illustrated by using the third-order pre-filter: following the same analyses described for N = 2, the high- and low-ripple peaks of the third-order pre-filter must coincide to provide a ripple-free input current i_g. However, to ensure that all the cells exhibit the same switching frequency, the switches of all the cells must be turned on and turned off once in each period. Therefore, because for N = 3 there are three inductor currents, two options are available: the first option considers the high peak of i_1 compensated with the low peak of i_2 (HP_1,LP_2), the high peak of i_2 compensated with the low peak of i_3 (HP_2,LP_3), and the high peak of i_3 compensated with the low peak of i_1 (HP_3,LP_1). The second option considers the compensations given by (HP_1,LP_3), (HP_2,LP_1) and (HP_3,LP_2).

Following the time shifting procedure performed in (6), the waveform of i_3 is obtained by shifting i_1 in $2\Delta T$ or by shifting i_2 in ΔT. Therefore, both operation options for N = 3 require three shift times ΔT in each switching period. Then, following the procedure described for N = 2, the two solutions given in (8) are obtained from $i_1+i_2+i_3-3I_1=0$ to ensure a null ripple in i_g. Both solutions require $\Delta T = T/3$.

$$\left\{\Delta T=D\cdot T \text{ with } D=\frac{1}{3}\right\} \quad or \quad \left\{\Delta T=\frac{D\cdot T}{2} \text{ with } D=\frac{2}{3}\right\} \quad (8)$$

Figure 4 shows the behavior of the third-order pre-filter with those solutions: both options provide the desired mitigation between the inductor current ripples to generate a ripple-free i_g.

The general expressions for the N-order pre-filter are obtained using the analysis previously described for N = 2 and N = 3. The expressions in (9) describe the optimal operating conditions for any number of cells N, where N-1 solutions could be adopted to mitigate the ripple in i_g. In addition, Table 1 presents the peak compensation generated in each optimal duty cycle for N = 5 and for a general N value. This table provides evidence of the multiple operation conditions available for a high-order pre-filter. Therefore, additional criteria are required to select a particular duty cycle among the options given in (9).

$$\left\{\Delta T=\frac{1}{N} \text{ with } D_{k,N}=\frac{k_{pf}}{N}\right\} \quad \forall\, k_{pf}=1,2\cdots N-1 \quad (9)$$

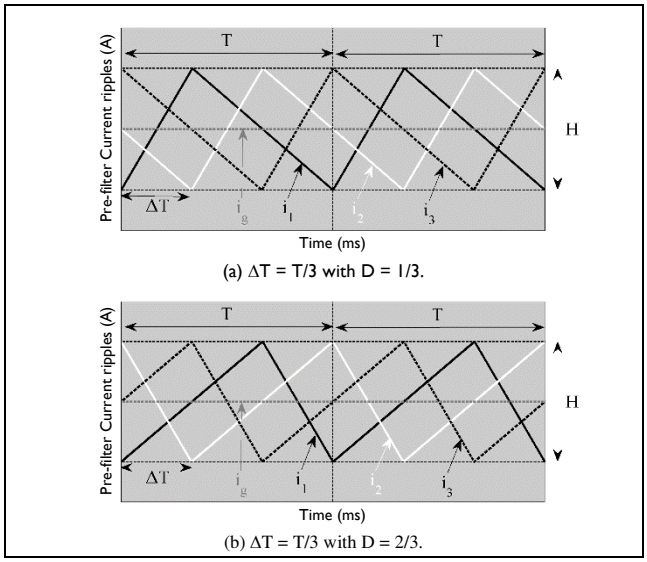

Figure 4. Behavior of the third-order pre-filter (N = 3)

Table 1. Peaks compensation for N=5 and for a general N value

$D_{k,N}$	Peaks compensation				
1/5	(HP_1,LP_2)	(HP_2,LP_3)	(HP_3,LP_4)	(HP_4,LP_5)	(HP_5,LP_1)
2/5	(HP_1,LP_3)	(HP_2,LP_4)	(HP_3,LP_5)	(HP_4,LP_1)	(HP_5,LP_2)
3/5	(HP_1,LP_4)	(HP_2,LP_5)	(HP_3,LP_1)	(HP_4,LP_2)	(HP_5,LP_3)
4/5	(HP_1,LP_5)	(HP_2,LP_1)	(HP_3,LP_2)	(HP_4,LP_3)	(HP_5,LP_4)
1/N	(HP_1,LP_2)	(HP_2,LP_3)	…	(HP_{N-1},LP_N)	(HP_N,LP_1)
2/N	(HP_1,LP_3)	(HP_2,LP_4)	…	(HP_{N-1},LP_1)	(HP_N,LP_2)
k/N	(HP_1,LP_{k+1})	(HP_2,LP_{k+2})	…	(HP_{N-1},LP_{k-1})	(HP_N,LP_k)
(N-1)/N	(HP_1,LP_N)	(HP_2,LP_1)	…	(HP_{N-1},LP_{N-2})	(HP_N,LP_{N-1})

Pre-filter voltage conversion ratio

Each optimal duty cycle available for an N-order pre-filter imposes a particular voltage conversion ratio $M(D)_{pf}$. These voltage conversion ratios are calculated from the single cell $M(D)_C$ given in (5) by accounting for the optimal duty cycles given in (9), which leads to the $M(D)_{pf}$ expression given in (10). It is noted that the higher the duty cycle, the higher the voltage conversion ratio. Therefore, the maximum voltage conversion ratio $M(D)_{pf,MAX}$ is achieved for k_{pf} = N-1 as given in (11). This expression considers all of the cells to be equal, i.e., $L_1 = L_k = L$ and $R_{L1} = R_{Lk} = R_L$, which is the correct approach to ensure that the cells have the same impedance to simplify the control design.

$$M(D)_{pf}=\frac{N\cdot k_{pf}}{N\cdot k_{pf}-k_{pf}^2+\left(R_L/Zi\right)\cdot N} \quad (10)$$

$$M(D)_{pf,MAX}=\frac{N-1}{1-\left(1/N\right)+\left(R_L/Zi\right)} \quad (11)$$

Figure 5 illustrates the $M(D)_{pf}$ for $2 \le N \le 7$, where it is confirmed that $M(D)_{pf,MAX}$ occurs at the maximum $k_{pf} = N-1$. In addition, it is observed that similar $M(D)_{pf}$ are obtained with different N values, e.g., N = 2, N = 4 with $k_{pf} = 2$, and N = 6 with $k_{pf} = 3$. However, higher N values require more complex and costly pre-filters, which suggests that $k_{pf} = N-1$ must be adopted.

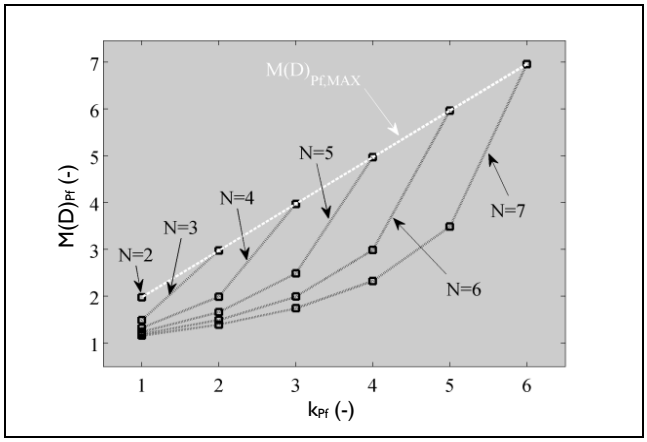

Figure 5. Pre-filter voltage conversion ratios

Finally, two characteristics must be noted: first, the correct operation of the pre-filter requires a cell current control; second, the pre-filter allows a classical Boost regulator to significantly increase the regulated voltage conversion ratio. Both characteristics are analyzed in detail in the following sections.

Programmed interleaved current control (PICC)

To ensure uniform current sharing among the cells, the programed interleaved current control (PICC) drives the switches to ensure a maximum difference between the pre-filter inductor currents. This strategy is similar to the hysteretic current control used in classical converters (Erickson and Maksimovic, 2001), but it is extended to several parallel cells.

The PICC detects the conditions for compensating the current ripples given in the last row of Table 1, accounting for the highest voltage conversion ratio. When these conditions appear, the cell's switches are configured to constrain the inductor's current difference. Figure 6 describes the implementation of the PICC for N cells: when the difference between the associated currents (as in Table I) is higher than the desired limit H, a comparator generates a trigger signal T_k. Then, a rules matrix defines the actions on the switches to avoid an increment in the current difference. For example, if $i_{k+1} - i_k \ge H$, i.e., $T_k = 1$, the control signal u_k of the MOSFET k is "Set" to force the increment of i_k, while the signal u_{k+1} of the MOSFET k+1 is "Reset" to force the decrement of i_{k+1}. This action ensures that $i_{k+1} - i_k \le H$, which effectively constrains the cells' current ripple. Finally, the state of the MOSFET control signal is stored in a Set-Reset flip-flop.

Because the MOSFETs must be switched in the same order given in the last row of Table 1 to guarantee the $M(D)_{pf,MAX}$, the switching rules T_k must be evaluated sequentially from T_1 to T_N. Therefore, T_k is considered if T_{k-1} was already triggered. This evaluation procedure could be easily implemented in a digital device using a digital hardware description, e.g., VHDL in an FPGA or by using a standard programming language, e.g., C language in a DSP or micro-controller. Finally, the adders, comparators and flip-flops are easily designed with classical analog components.

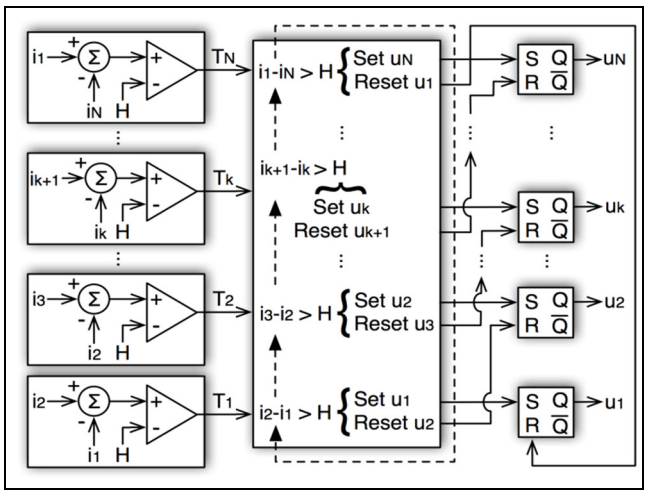

Figure 6. Programmed interleaved current control (PICC)

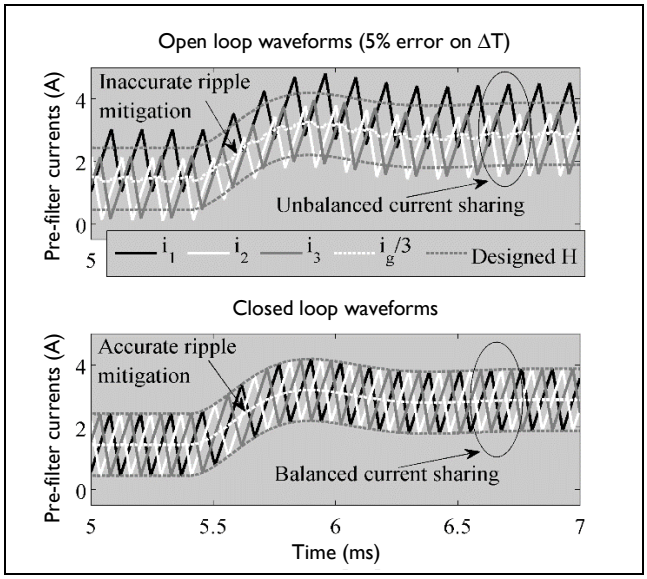

Figure 7. PICC performance for N = 3

Figure 7 shows the operation of a third-order pre-filter with the following cell parameters: $L_1 = L_k = L = 1$ mH, $R_{L1} = R_{Lk} = R_L = 50$ mΩ, $C_P = 6.8$ μF and $Z_i = 50$ Ω. The simulation also considers $V_g = 24$ V, H = 0.8 A and a load perturbation at t = 5.4 ms to $Z_i = 25$ Ω. The upper traces of Figure 7 consider an open loop operation with a constant duty cycle (11) and a fixed shift time ΔT because the element tolerances and aging exhibit an error of 5 %. The simulation results show that this small error generates significant differences in the average currents, which deteriorates the ripple mitigation and overcharges a cell. Instead, the bottom traces of Figure 7 consider the action of the PICC, where the cell ripples are constrained to the desired H magnitude, ensuring balanced current sharing among the cells and providing a satisfactory ripple-free input current. A similar condition is obtained for small differences in the cells' parameters: in a closed loop, the cells' ripples are constrained, while in an open loop, several differences appear.

Pre-filter-based regulators

As previously described, the pre-filter filters the current harmonics generated by classical regulators, and at the same time, it improves the Boost regulator characteristics. The pre-filter is connected in series with the Boost regulator as shown in Figure 2.

Therefore, the load impedance interacting with the pre-filter is the input impedance of the Boost regulator.

Moreover, the voltage conversion ratio and efficiency of this series connected regulator, called the pre-filter-based regulator, depend on both the pre-filter and the regulator. Therefore, the following subsections review the classical Boost regulator characteristics to analyze the pre-filter-based regulator.

Classical Boost Regulator characteristics

The classical boost regulator (CR) depicted in Figure 1 transforms the source power to the supply regulated power to the load R. To provide a fair comparison, the CR is considered along with the same elements adopted for the pre-filter. In practice, this is the worst case because smaller inductors could be used for the pre-filter, exhibiting lower losses and improving the efficiency.

The CR voltage conversion ratio is given in (12), while the average inductor current is given in (13) (Erickson and Maksimovic, 2001). Similarly, considering the power losses P_{LCR} that occur in R_L, the CR efficiency is given in (14). Finally, the CR input impedance, i.e., the pre-filter load, is given in (15).

$$M(D)_{CR} = \frac{(1 - D_{CR})}{(1 - D_{CR})^2 + (R_L / R)} \tag{12}$$

$$I_{CR} = \frac{V_g / R}{(1 - D_{CR})^2 + (R_L / R)} \tag{13}$$

$$\eta_{CR} = 1 - \frac{P_{LCR}}{V_g \cdot I_{CR}} \quad , \quad P_{LCR} = I_{CR}^2 \cdot R_L \tag{14}$$

$$Zi = \left[(1 - D_{CR})^2 + (R_L / R) \right] \tag{15}$$

Pre-filter-based regulator characteristics

From the pre-filter-based (Pf-R) scheme of Figure 2, the following electrical characteristics hold: the cells exhibit an average current $I_1 = I_2 = I_K = I_S$, where I_S represents the average current of the CR inductor generated by its interaction with the pre-filter and the load. This condition is deduced from the average current of the pre-filter diodes, $I_D = I_S/N$, which leads to the average inductor currents $I_k = I_D/(D_{k,N}) = N \cdot I_D = I_S$.

The Pf-R voltage conversion ratio M(D) is given in (16), where Zi in (11) is given by (15). Similarly, from (11) and (13), the inductor average currents (cells and CR) are given by (17), where D_S represents the CR duty cycle required in the Pf-R solution.

$$M(D) = M(D)_{pf,MAX} \cdot M(D)_{CR} \tag{16}$$

$$I_S = I_k = \frac{V_g / R}{\frac{(1 - D_S)^2 + (R_L / R)}{N} + \frac{(R_L / R)}{N - 1}} \tag{17}$$

Then, the efficiency and power losses on the Pf-R circuit are given in (18). To contrast the power losses on both CR and Pf-R circuits, the improvement losses ratio $\beta_{pf\text{-}R/CR}$ is defined in (19). Because $\beta_{pf\text{-}R/CR} < 1$ for $N \geq 2$, it is evident that the pre-filter-based regulator has a higher efficiency in comparison with the classical Boost regulator.

$$\eta_{pf-R} = 1 - \frac{P_{Lpf-R}}{V_g \cdot I_g} \quad , \quad P_{Lpf-R} = (N+1) \cdot I_S^2 \cdot R_L \tag{18}$$

$$\beta_{pf-R/CR} = \frac{P_{LCR}}{P_{Lpf-R}} = \frac{N+1}{N^2} < 1 \tag{19}$$

Figure 8 shows the simulation of both Pf-R and CR circuits for different M(D) conditions. The simulations consider the same parameters described in the previous section. The results show that the Pf-R solution can provide the same M(D) as the CR solution but with an improved efficiency, e.g., for M(D) = 4, the Pf-R with N = 2 improves by 6.1 % of the regulator efficiency, while the Pf-R with N = 3 improves the efficiency by 15.4 %. Moreover, the Pf-R solution allows higher voltage conversion ratios that are not achievable by CR alone, e.g., with N = 3, the Pf-R provides M(D) = 6 with an efficiency equal to 90 %, and the Pf-R with N = 5 provides a maximum M(D) = 16.7, while the maximum M(D) for the CR is 5.0. These results provide evidence of the significant improvement in the efficiency and voltage conversion ratio generated for the classical Boost regulator by the pre-filter operation.

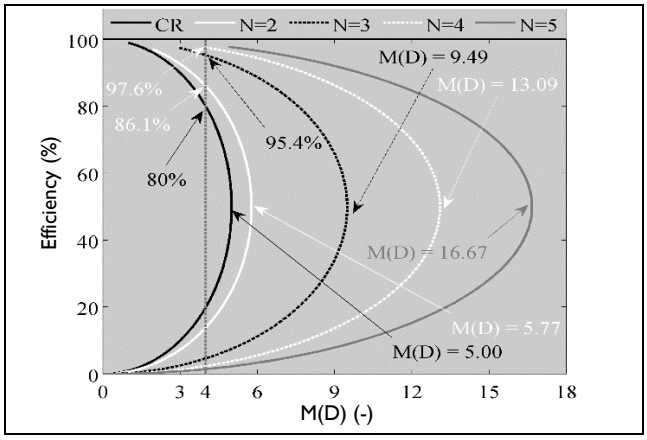

Figure 8. Pre-filter-based regulators efficiency and M(D)

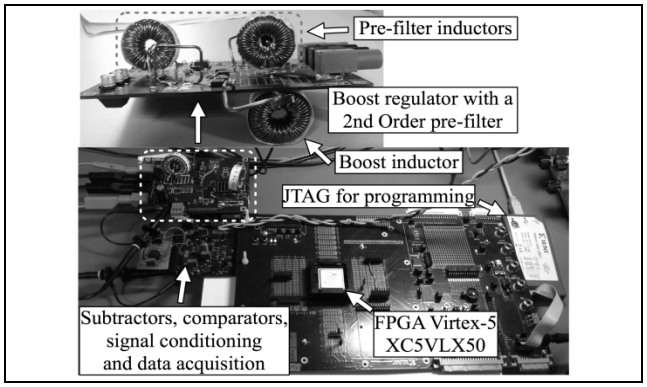

Figure 9. Experimental test bench with N = 2

Experimental results

To experimentally validate the proposed solution, the *proof-of-concept* prototype depicted in Figure 9 was developed. This prototype consists of a second-order pre-filter interacting with a classical Boost regulator. The prototype is controlled with a Virtex-5 FPGA that is programmed using a JTAG device. Moreover, the comparators and adders were implemented with analog circuitry.

Figure 10 shows the pre-filter-based waveforms at both high (top) and low (bottom) load current conditions: because the Boost regulator operates in a continuous conduction mode (CCM in top) or in a discontinuous conduction mode (DCM in bottom), the pre-filter cell currents are accurately shifted to provide a ripple-free input current. Moreover, because the tolerances of the cells' elements generate some differences among the cells' impedances, the input current does not exhibit a significant ripple because of the correctness of the proposed controller.

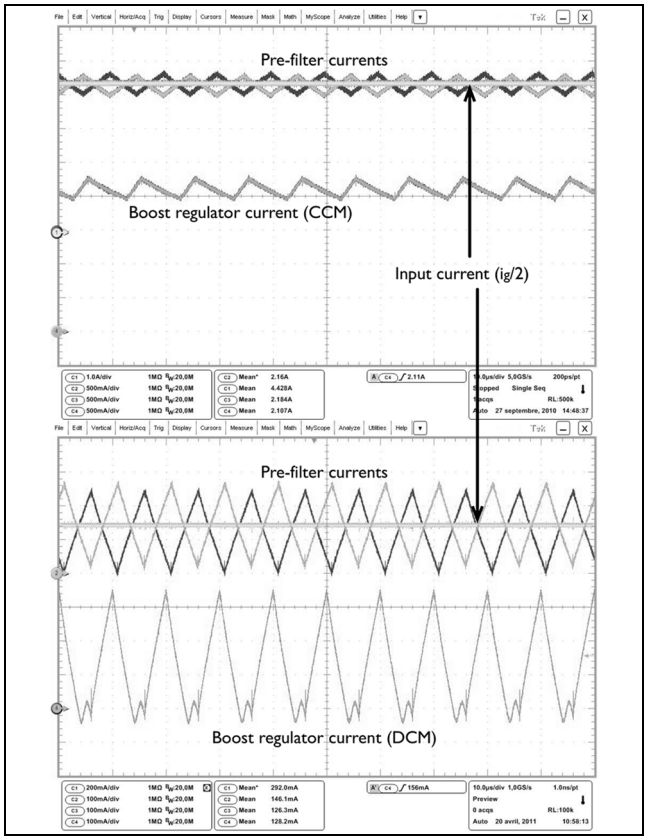

Figure 10. Experimental waveforms at both high- and low-load current

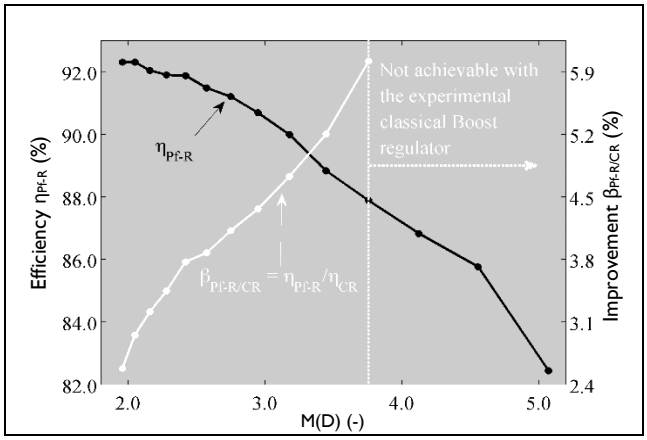

Figure 11. Experimental efficiency and M(D)

Figure 11 shows the experimental efficiency $\eta_{pf\text{-}R}$ of the pre-filter-based regulator for different M(D) conditions. In addition, the figure presents the experimental losses ratio $\beta_{pf\text{-}R/CR}$, where the efficiency improvement provided by the pre-filter to the classical Boost regulator is observed. Similarly, the M(D) conditions that are not achievable with the CR prototype but are achievable with the Pf-R prototype are also highlighted.

Finally, these experimental results validate the analytical and simulation results presented previously. The experiments illustrate the benefits of introducing the proposed pre-filter structure between the source and the regulator: current harmonics filtering, improved efficiency and higher voltage conversion ratio.

Conclusions

An active pre-filter was proposed to protect the source from the regulators' current ripples. The pre-filter also increases the overall efficiency and achieves higher voltage conversion ratios. Moreover, the pre-filter provides the same voltage conversion ratio as the classical solutions but with an improved efficiency. In addition, the pre-filter does not affect the main regulator control. Similarly, the pre-filter's main drawback consists in an increased number of elements, which increases the solution size and cost. Furthermore, modern drivers with diode-MOSFET synchronization or even synchronous boost topologies are desirable to avoid the commutation problems among the pre-filter branches in practical implementations.

Finally, the proposed solution is a suitable option for improving the characteristics of the classical Boost regulators dedicated to low-ripple/high-boosting applications, such as photovoltaic and fuel cell power systems.

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